Digitally Assisted Analog Electronics : Trade-offs and Applications on Mixed Signal and RF Front-ends

Vom Fachbereich 18
Elektro- und Informationstechnik Institut für Datentechnik
der Technischen Universität Darmstadt
zur Erlangung des akademischen Grades eines
Doktor-Ingenieurs (Dr.-Ing.)
genehmigte Dissertation

von

M.Sc.
Botao Xiong
geboren am 06. March 1987
in Gansu, China

Referent: Prof. Dr.-Ing. Klaus Hofmann
Technische Universität Darmstadt

Korreferent: Prof. Dr.-Ing. Thomas Hollstein
Tallinn University of Technology

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Erklärung zur Dissertation

Hiermit versichere ich, die vorliegende Dissertation ohne Hilfe Dritter nur mit den angegebenen Quellen und Hilfsmitteln angefertigt zu haben. Alle Stellen, die aus Quellen entnommen wurden, sind als solche kenntlich gemacht. Diese Arbeit hat in gleicher oder ähnlicher Form noch keiner Prüfungsbehörde vorgelegen.

Darmstadt, den

(Botao Xiong)

Acknowledgment

This dissertation is based on my work that I have started in Oct 2012 at integrated electronic system lab, TU Darmstadt as a four-year scholarship student.

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Last but not the least, I would like to dedicate this dissertation to my parents for their love, understanding and selfless support in all my pursuits. Without your help in my personal life, I could not focus on my study and research. Thank you.

Darmstadt, Jun 2016

Botao Xiong

Abstract

The development of integrated circuits has been governed by $Moore^{'}s$ law for several decades. Through continuous advancements in CMOS technology, the industry has maintained exponential progress rates in transistor miniaturization and integration density. However, this technology scaling trend is only conditionally beneficial for analog circuit performance. Compared with the analog circuits, digital circuits are cheaper, faster, more complex, and more power efficient. Due to these reasons, the researchers are undertaking a paradigm shift from high performance analog circuits to digitally assisted analog circuits.

Adaptive impedance matching techniques are attractive because they provide resilience to antenna impedance variation caused by body-effects and several other reasons. In principle, they can preserve maximum radiated power, power amplifier linearity, receiver sensitivity, and power efficiency of a mobile phone simultaneously. However, achieving proper adaptive impedance control over a large impedance region is a challenge.

Recent analog and RF circuits are increasing performance and efficiency with the aid of digital technology. To apply this technique to a reconfigurable antenna system, a fully integrated micro-controller based on AMS H35 technology has been designed. Digital calibration blocks wrapped around an analog core are capable of performing dead time and impedance matching schemes. Therefore, the intelligence and robustness of the system are improved significantly. Furthermore, compared with S11 controller (18.8mm^2, 186mW), the silicon area of the digitally assisted circuit (4mm^2, 62mW) is acceptable.

In addition, this dissertation presents a set of convergence criteria for the tunable matching network, which leads to the finding of matching point with high probability. Furthermore, to accelerate the convergence speed, the binary search tuning algorithm has been proposed. In contrast to the single step method, the tuning speed is improved from *O(N)* to *O(log(N))*.

Kurzfassung

Die Entwicklung integrierter Schaltkreise wurde jahrzehntelang durch das Mooresche Gesetz geregelt. Durch ständige Weiterentwicklungen in der CMOS-Technologie erreicht die Branche exponentielle Fortschritte in der Miniaturisierung von Transistoren und der Integrationsdichte. Der Skalierungstrend dieser Technologie ist für die Leistung analoger Schaltkreise jedoch nur bedingt von Vorteil. Im Vergleich mit analogen Schaltkreisen sind digitale Schaltkreise billiger, schneller, komplexer und energieeffizienter. Aus diesen Gründen haben die Forscher einen Paradigmenwechsel von analogen Hochleistungsschaltkreisen hin zu digital unterstützten analogen Schaltkreisen vollzogen.

Die Techniken der adaptiven Impedanzanpassung sind attraktiv, weil sie widerstandsfähig gegenüber den Impedanzschwankungen der Antenne sind, die durch Körpereffekte und einige andere Gründe verursacht werden. Prinzipiell können sie die maximale Strahlungsleistung, die Linearität der Leistungsverstärker, die Empfängerempfindlichkeit und die Energieeffizienz eines Mobiltelefons gleichzeitig erhalten. Die Herausforderung besteht jedoch darin, die korrekte adaptive Impedanzkontrolle über einen groβen Scheinwiderstandbereich zu erreichen.

Moderne analoge und HF-Schaltungen steigern die Leistung und Effizienz mit Hilfe digitaler Technologie. Zum Einsatz dieser Technik bei einem rekonfigurierbaren Antennensystem wurde ein auf AMS H35-Technologie basierender, vollständig integrierter Mikrocontroller konstruiert. Digitale Kalibrierblöcke, die um einen analogen Kern herum angeordnet sind, ermöglichen die Durchführung von Totzeit sowie Impedanzanpassung. Auf diese Weise werden die Intelligenz und die Robustheit des Systems deutlich verbessert. Zudem bleiben im Vergleich mit einem S11-Controller (18.8mm^2, 186mW) der Siliziumbereich der digital assistierten Schaltung(4mm^2, 62mW) in einem akzeptablen Rahmen.

Des Weiteren präsentiert diese Abhandlung eine Reihe unimodaler Kriterien für das abstimmbare Anpassungsnetzwerk, die es erlauben, den Punkt des globalen Optimums zu finden mit hoher Wahrscheinlichkeit. Darüber hinaus dient ein binärer Suchabstimmalgorithmus zur Erhöhung der Konvergenzgeschwindigkeit. Im Gegensatz zur Einzelschritt-Methode verbessert sich dabei die Abstimmgeschwindigkeit von O(N) auf O(log(N)).

Table of Contents

List of Tables

List of Figures

List of Abbreviations

RF	:	Radio Frequency
UMTS	:	Universal Mobile Telecommunications System
GSM	:	Global System for Mobile communications
EDGE	:	Enhanced Data rates for GSM Evolution
GPS	:	Global Positioning System
VCO	:	Voltage-controlled Oscillator
LNA	:	Low-Noise Amplifier
PA	:	Power Amplifier
WLAN	:	Wireless Local Area Network
TMN	:	Tunable Matching Network
MEMS	:	Micro-Electro-Mechanical System
ASIC	:	Application-Specific Integrated Circuit
BCD	:	Bipolar-CMOS-DMOS
SOI	:	Silicon-on-Insulator
SoC	:	System-on-Chip
CMOS	:	Complementary Metal-Oxide-Semiconductor
IC	:	Integrated Circuit
CGA	:	Conventional Genetic Algorithm
QGA	:	Quantum Genetic Algorithm
LFT	:	Linear Fractional Transformation
BST	:	Barium Strontium Titanate
DRA	:	Dielectric Resonator Antenna
DPWM	:	Digital Pulse Width Modulator
RISC	:	Reduced Instruction Set Computing
NVIC	:	Nested Vectored Interrupt Controller
DAA	:	Digitally Assisted Analog
SDR	:	Software Defined Radio

DFS	:	Dynamic Frequency Scaling
CPU	:	Central Processing Unit
RAW	:	Read After Write
WAR	:	Write After Read
WAW	:	Write After Write
DFS	:	Dynamic Frequency Scaling
LCD	:	Liquid-crystal Display
FPGA	:	Field Programmable Gate Array

Chapter 1

Introduction

Contents

1.1 Background

Mixed signal applications are among the fastest growing segments in the electronics industry requiring a high integration of analog and digital circuits. However, the analog design is significantly lagging behind the development of digital designs. Over the past decades, (1) The number of transistors per die has doubled every two years resulting in a tremendous improvement in the computing power of digital circuits. (2) The energy per logic operation has been reduced significantly. For example, a 2-input NAND gate dissipates 1.3pJ per logic operation in 0.5μm CMOS technology. However, the same gate dissipates 4.5fJ in 90nm technology [1]. As shown in Fig.1.1, in the case of 0.25μm technology, the power consumption of a 16-bit ADC is approximately equal to the Cortex-R4 processor. (3) Analog circuits are constrained by electronic noise, linearity and matching requirements. Fortunately, the linearity and matching can be assisted by digital circuits. The basic ideas are digital calibration and digital compensation.

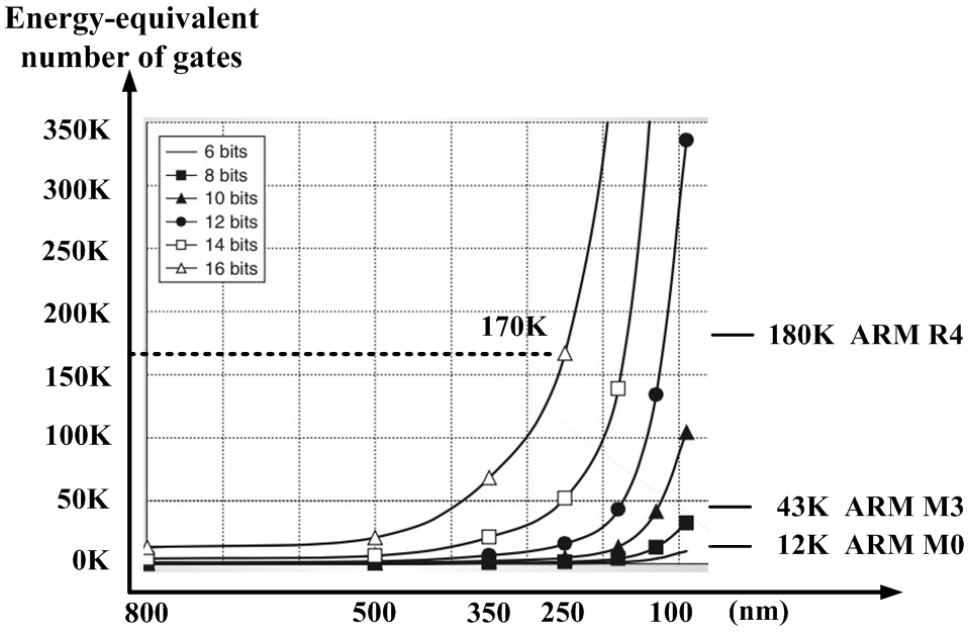

Fig. 1.1: Energy-equivalent number of logic gates [2]

1.2 State-of-the-Art

1.2.1 Digitally Assisted AD Converter

As shown in Fig.1.2, a conventional, high performance, high power ADC is replaced by a low performance, low power ADC, followed by a digital post-processor, which can calibrate the output to achieve the same accuracy. Compared with the conventional ADC, the digitally assisted ADC has a significant benefit in terms of power and area. This method is referred to as digital calibration.

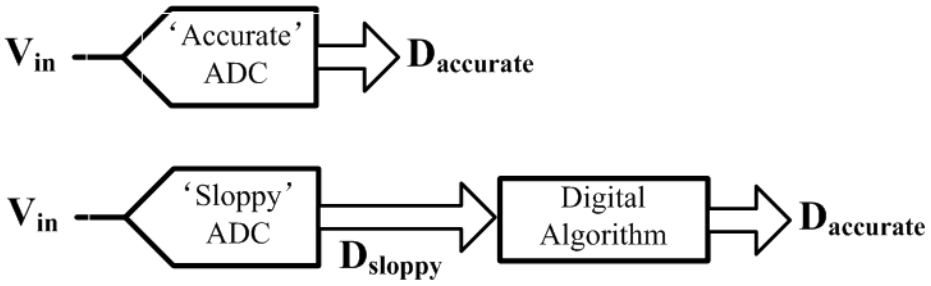

Fig. 1.2: Digitally assisted ADC [2]

1.2.2 Digitally Assisted Power Amplifier

As shown in Fig.1.3, the non-linear distortion in power amplifiers can be improved by pre-distorters. Because the power amplifier is memoryless and there is no filter between the predistorter and the power amplifier, it is sufficient to use a memoryless data predistorter here. The predistorter can be easily implemented as look-up tables (LUTs) that map the original input constellation points to the desired locations. This method is referred to as digital compensation.

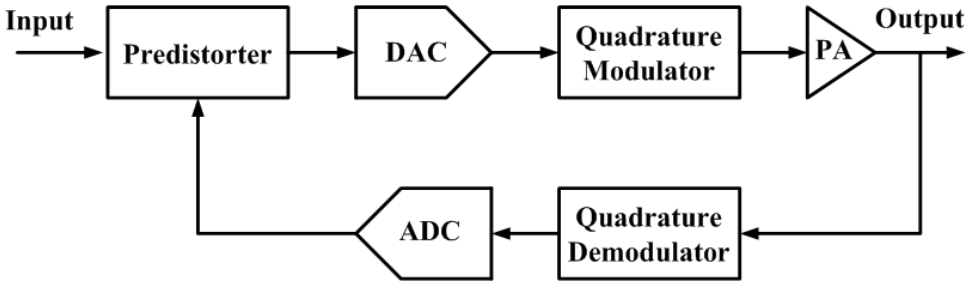

Fig. 1.3: Block diagram of a data predistortion system [11]

1.2.3 Digitally Assisted Frequency Synthesizers

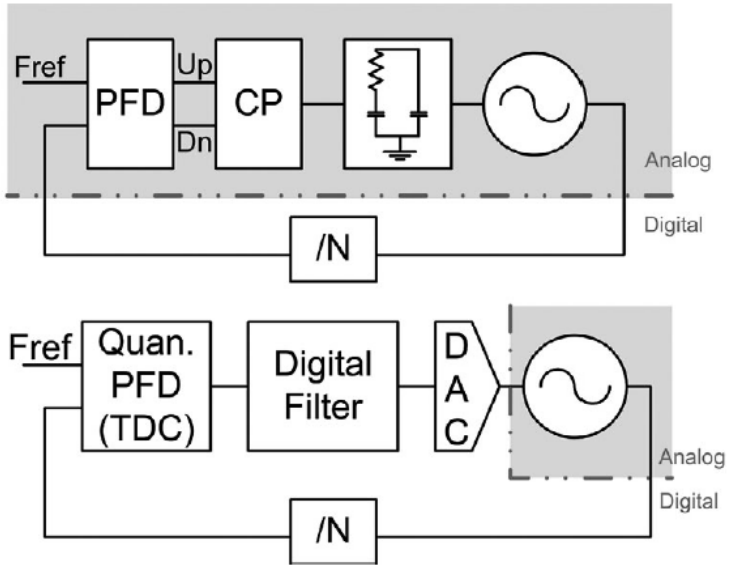

Fig. 1.4: Conceptual block diagrams of analog PLL and digital PLL [9, Chapter 4]

As shown in Fig.1.4, the analog PLL processes the phase information in the analog domain with a phase frequency detector and a charge pump circuit, so that the phase difference turns into current pulses. This current signal is converted into voltage with an

analog loop filter. Some digitally assisted concepts were adopted [3,4,5]. The key difference from an analog PLL is that it processes the phase information in the digital domain instead of the analog. Furthermore, because the PLL loop filter is entirely implemented by the digital filter, the die area is substantially reduced, and the frequency response is highly reconfigurable and insensitive to any manufacturing variability. Despite those advantages, compared to the charge pump architecture, a digital PLL requires additional overheads, which are the interface circuits between the analog and digital domain. For example, the phase frequency detector (PFD) is replaced by the time-to-digital (TDC). This converter consumes extra power and area, and adds time quantization noise to the PLL loop. Therefore, there has been strong design community interest in reducing the overhead of TDC in terms of both implementation cost and performance degradation [9].

1.2.4 Digitally Assisted Power Converters

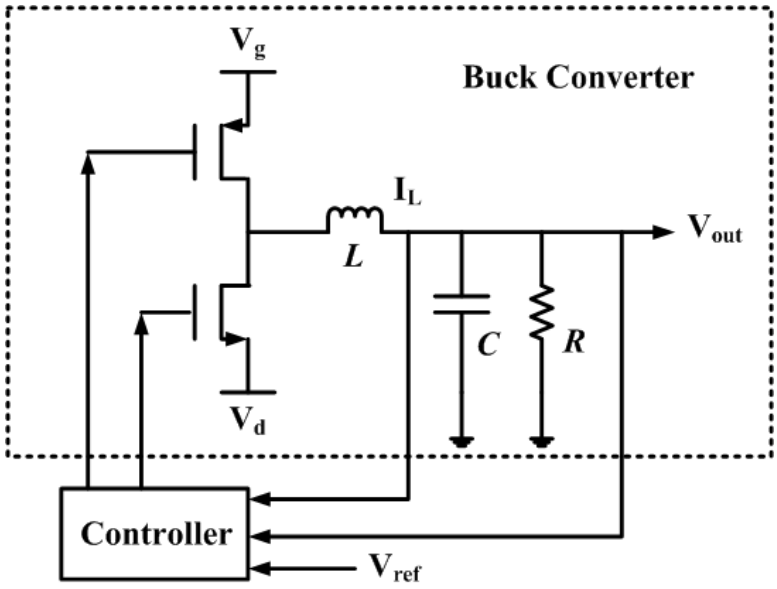

Fig. 1.5: A buck converter and a controller [9, Chapter 9]

A buck converter system consists of two parts. One is the buck converter itself and the other is a feedback controller, which is used to force the output voltage of the buck converter to be equal to the reference voltage regardless of the PVT variations and dynamic load. This is achieved by adjusting the duty cycle of the clock signal with the feedback information of the output voltage and inductor current. The controller is referred to as ”voltage-mode control” if only the output voltage is used as a feedback signal. It is called ”current-mode control” if both the output voltage and inductor current are used as the feedback signals. More details regarding the basic operations of digitally assisted buck converter systems can be found in [10]. In addition, a similar concept has been used in the RF design [6,7,8].

1.2.5 Digitally Assisted RF front-end

Tunable RF front-ends can be designed to adapt to different operating conditions, such as multiple frequency bands, antenna impedance variation and changing environment. As a result, tunable RF front-ends not only enhance the functionality and performance of communication system but also reduce the circuit size and cost.

The tunable matching networks originate from the fixed matching networks, which are used to transform the load impedance to the source impedance. All components of the fixed network cannot be changed after fabrication. Hence, tunable components are indispensable building blocks for tunable matching networks. The technologies of different tunable components are compared in section 2.2.1. The tunable matching networks have been used in the tunable power amplifier, tunable filters and antenna impedance variation.

The RF switches based tunable matching networks and corresponding adaptive impedance matching algorithms are investigated in [12,13]. Furthermore, this dissertation investigates the ferroelectric varactor based tunable matching network. Compared with the [13], this work achieves some significant advancements: (1) a fully integratable 4-phase charge pump has been verified in AMS H35 CMOS technology, which can provide a high tuning voltage (beyond 110V); (2) presents a novel adaptive impedance matching algorithm, which can be performed by Cortex-M0 controller in microseconds. The advantage of proposed system is fast tuning speed. In general, the antenna impedance variation can be calibrated in milliseconds. However, since this varactor requires a high tuning voltage (90V), the power consumption of this system is high (200mW). In addition, the chip size of charge pump ($18mm^2$) is large due to a large number of stages. As a result, the proposed system is a good solution for vehicle communication systems rather than mobile phones.

1.3 Research Objective

The above examples illustrate that researchers are undertaking a paradigm shift from high performance analog circuits to digitally assisted analog circuits. According to the preceding discussion, this dissertation applies the same ideas to charge pumps and tunable matching networks, which can be used in a reconfigurable antenna system.

The conventional charge pump cannot maintain its output voltage at the desired level due to the PVT variations and the dynamic load resistor. The unstable output voltage could reduce the performance of the system. In addition, the non-ideal clock switches could result in a conduction path. As a result, the reversion current will reduce the power efficiency. This dissertation utilizes a micro controller performing an adaptive 4-phase clock scheme to stabilize the output voltage and improve power efficiency.

A tunable matching network is used to calibrate the antenna impedance variation. By

performing the adaptive impedance matching algorithm, the proposed micro controller can minimize the return loss. In addition, the linearity of varactors can be improved by digital compensation technology.

In the end, this dissertation compares digitally-assisted analog circuits with pure analog circuits from the following perspectives: (1) power consumption, (2) chip size, (3) robustness, and (4) design effort.

1.4 Thesis Outline

The organization of this dissertation is summarized as follows:

- *Chapter 2:* Introduction of the application background, the charge pump and tunable matching network specifications.
- *Chapter 3:* Presentation of a set of convergence criteria for tunable matching networks and corresponding adaptive impedance matching algorithms.
- *Chapter 4:* Introduction of the mathematical model of a charge pump, such as the input-output relationship, and power efficiency. Presentation of the adaptive 4-phase clock algorithm. Discussion of the hybrid DPWM based 4-phase clock generator.
- *Chapter 5:* Evaluation of the proposed system from four perspectives: (1) power consumption, (2) chip size, (3) robustness, and (4) design effort. Discussion of the trade-offs on digital calibration and compensation.
- *Chapter 6:* Summary of the contributions of this dissertation.

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Chapter 2

Reconfigurable Antenna System

Contents

2.1 Background

Today, the communication device has to support multiple standards and adapt to the changing environment [1,2]. Therefore, tunable RF Front-ends are highly desired. As shown in Fig.2.1, a smart phone has to offer wireless connectivity in addition to the typical cellular phone service. A straightforward solution is to integrate multiple transceiver units into a single RF device. As shown in Fig.2.2, the tunable RF transceiver is an alternative solution for increasing hardware flexibility and functionality.

- *Multi-Frequency-Bands*: Wireless communication has evolved from a single mode, triple-band 2G system to a triple-mode, 9-band, high-speed data-capable system. The operation of multi-modes and multi-bands is performed by multiple stacked transceivers. To reduce the circuit size, tunable RF Front-ends supporting multiple standards in a single transceiver unit were proposed [3,4,5,6,7].
- *Received-Signal-Strength*: The performance of an RF receiver varies widely with the strength of the received signal. Hence, the RF Front-ends should adapt to the changing strength of the received signal [1,8].

- *Transmit-Power-Level*: The power amplifier (PA) operates at varying power levels due to the distance between the communicating base station and the hand-held device. By adjusting the biasing voltage/current [9,10] or load impedance [11,12] of the power amplifier, the overall power efficiency can be improved [13,14,15].
- *Fluctuating-Radio-Environment*: It is well-known that the antenna impedance is sensitive to nearby objects and human bodies. Therefore, an antenna tuning unit that can detect the antenna impedance variation and calibrate the tunable matching network (TMN) in real time is highly desired [16,17].

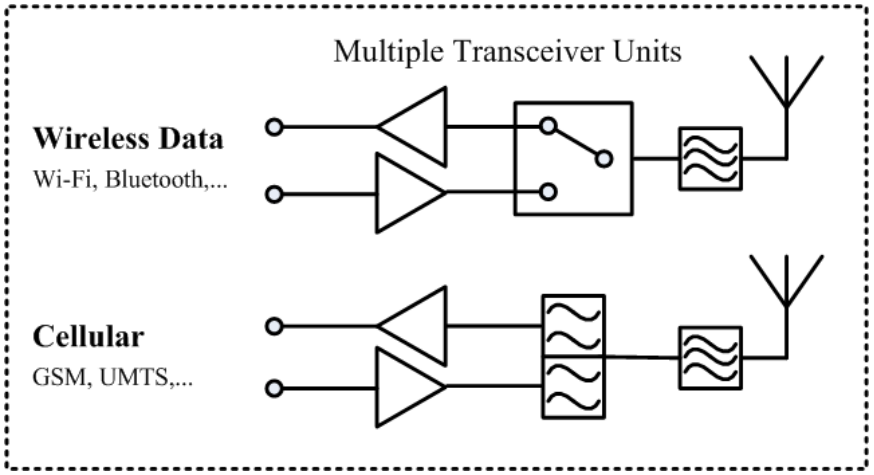

Fig. 2.1: A smart phone with multiple transceiver units

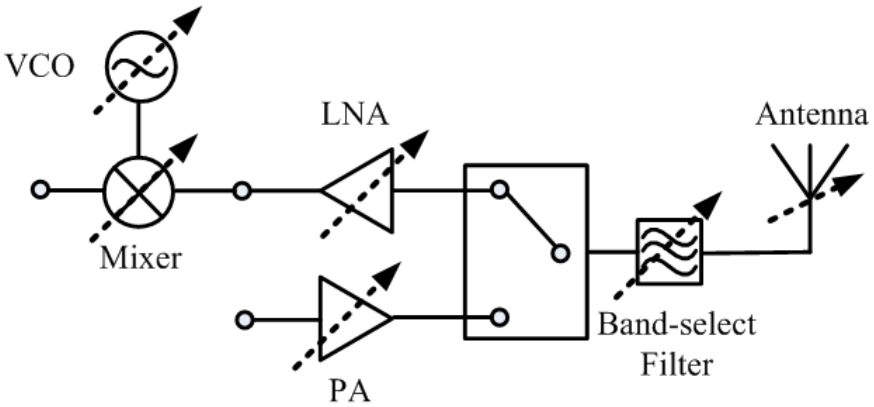

Fig. 2.2: Block diagram of an adaptive RF front-end module

2.2 Antenna Tuning Unit based on Functional Materials

2.2.1 Varactor Technologies

Tuning elements are indispensable building blocks for tunable matching networks. As shown in Fig.2.3, varactor technologies fall into three categories: semiconductor-based varactor diodes, microelectromechanical system (MEMS) varactors, and ferroelectric-based varactors. A performance comparison of these three varactor technologies is summarized in Tab.2.1 [18,19,20]. A tunable T-type matching network based on ferroelectric technology has been fabricated that requires a high tuning voltage (beyond 100V). However, high tuning voltage is a challenge for portable devices.

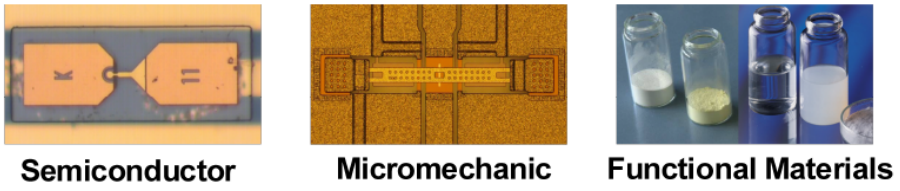

Fig. 2.3: Three Varactor Technologies [18]

Tab. 2.1: Comparison of different varactor technologies

	Semiconductor-based	MEMS	Ferroelectric-based
Tunability	high	low	medium
Quality Factor	medium	high	medium
Bias Voltage	medium	high	medium
Tuning Speed	fast	slow	fast
Power Handling	low	medium	high
Linearity	can be improved	high	can be improved

2.2.2 High Voltage ASICs

In the past, the CMOS technology was limited to low voltage domains (below 5V). High voltage domains were dominated by BCD (Bipolar-CMOS-DMOS) and SOI (Silicon-on-Insulator) technologies. In recent years, high voltage CMOS technology became a reality [21,22,23,24]. The minimum feature size of high voltage CMOS technology has decreased from 0.8um to 0.18um [25,26,27,28,29].

2.2.3 Functional Specification

Functional materials [31,32,33,34] can be used to provide tunability for mobile devices. To reduce the mismatch between the antenna and matching network [30], a reconfigurable dual-band antenna system is introduced in this section. The block diagram of this system is depicted in Fig.2.4.

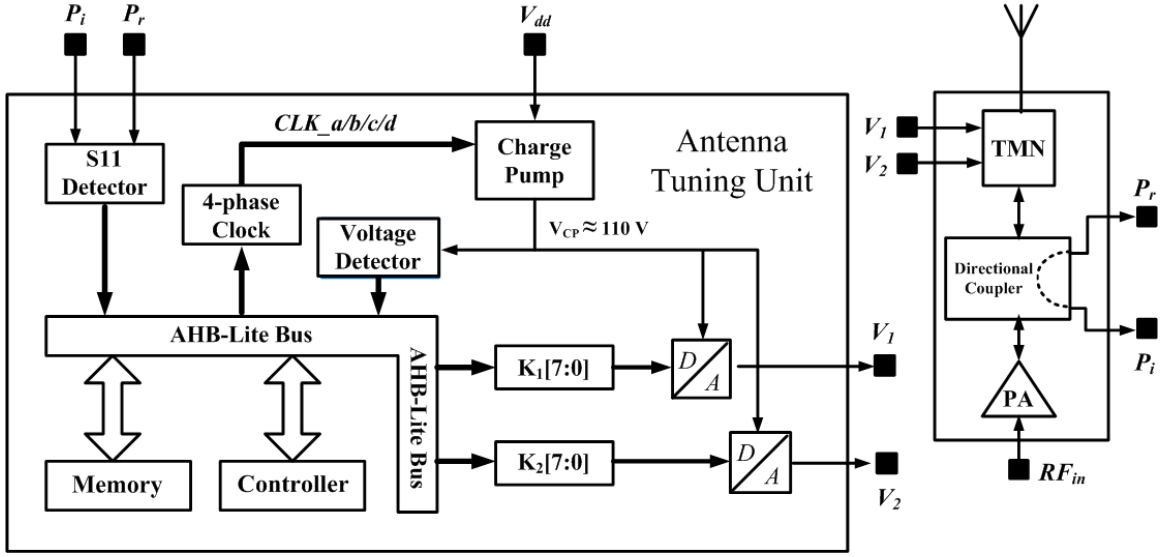

Fig. 2.4: Architecture of reconfigurable dual-band antenna system

This system consists of a dual-band antenna [35,36,37,38], a tunable T-type matching network [38,39,40], a charge pump [41,42,43], two HV-DACs [44], an S11 detector, a voltage detector, and a micro-controller. The dualband hybrid dielectric resonator antenna (DRA) covering the 1.9GHz and 5.1GHz bands was fabricated [38,45]. The tunable T-type matching network proposed in [38,40] was employed to reduce the return loss. The two varactors vary their capacitance from 0.31pF to 0.22pF according to the tuning voltage ranging from 0V to 90V. The maximum output voltage of the charge pump is 120V because the supply voltage of HV-DAC is 110V.

2.2.4 Design Considerations

The first concern is that the output voltage of the charge pump is affected by the PVT variations and changing load impedance. In addition, the mismatch between the antenna and tunable matching network will result in a large reflection power, which will decrease the performance of communication devices. This dissertation aims to solve these two problems with digitally assisted techniques.

2.3 References

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Chapter 3

Tuning Method of Tunable Matching Network

Contents

3.1 State of the Art

Adaptive impedance matching techniques are attractive because they provide resilience to antenna impedance variation caused by body-effects and several other reasons [5]. In principle, they can preserve maximum radiated power, power amplifier linearity, receiver sensitivity, and power efficiency of a mobile phone simultaneously. However, achieving proper adaptive impedance control over a large impedance region is a challenge [6,14].

The simplest and fastest tuning method is the single step algorithm [1,7]. Gradient-based algorithms involve large computational burden since they require to calculate the gradient of the objective function [2]. A common disadvantage of these approaches is that all algorithms are easily trapped into a local optimum point. To reach the global optimum point, some evolutionary optimization algorithms, such as conventional genetic algorithm (CGA), quantum genetic algorithm (QGA), have been employed [8,9,10]. To secure reliable convergence, a cascade of two control loops is proposed [11]. Additionally, by measuring the load impedance, a novel direct calculation method for matching network is presented in [12]. The matching region of Π-type network is analytically calculated in [13]. The antenna impedance variation located in the matching region is likely to be calibrated. However, as long as the objective function has multiple local optimum points, there is no guarantee in theory that the optimization algorithms are capable of converging to the global optimum point.

To solve preceding problems, design strategies of T-type and Π-type network are presented. In contrast to the traditional approaches, the proposed convergence criteria ensures that we are most likely to converge to the neighbourhood of matching point, which has been proven in Appendix D.

In case of matching network with fixed X_1, the proposed convergence criteria ensure that the input resistance is proportional to the tunable X_2 and input reactance is proportional to the tunable X_3. Similarly, in case of matching network with fixed X_2, the input resistance is proportional to the tunable X_1 and input reactance is proportional to the tunable X_3 . As a result, the binary search algorithm is employed to accelerate the convergence speed. In contrast to the single step method [1], the tuning speed is improved from *O(N)* to *O(logN)*.

This chapter is organized as follows. The mathematical properties of Γ-type matching network are investigated in section 3.2. The convergence criteria and design strategies of T-type and Π-type matching network are discussed in section 3.4 and 3.5, respectively. The binary search tuning algorithm is proposed in section 3.6. Some concerns about lossy matching network are solved in section 3.8.

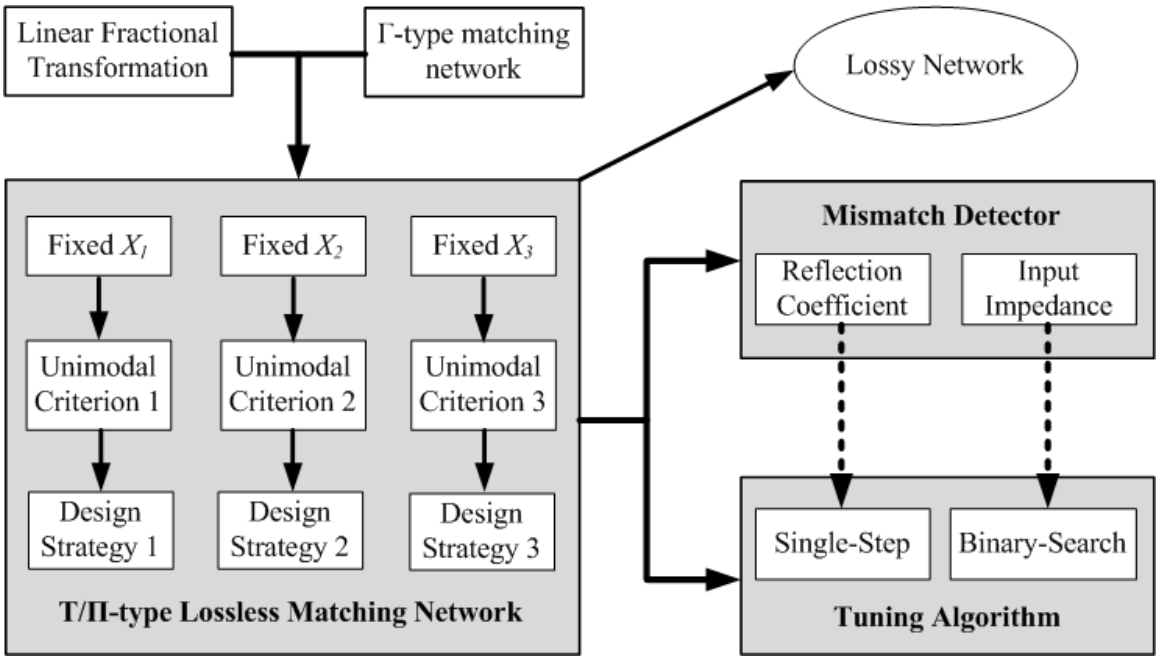


Fig. 3.1: Structure of Chapter 3

3.2 Mathematical Properties of Γ-type Network

3.2.1 Linear Fractional Transformation (LFT)

We begin our discussion with a brief introduction to the linear fractional transformation, which plays an important role in this work. If *a*, *b*, *c*, and *d* are complex constants with *ad-bc*$\neq$*0*, then the complex function (3.1) is called a linear fractional transformation.

$$w = \frac{a \times z + b}{c \times z + d} \tag{3.1}$$

A linear fractional transformation maps a circle or a line in the *z*-plane to either a line or a circle in the *w*-plane. The image is a line if and only if the original circle or line passes through a pole of the linear fractional transformation. The central point and radius are calculated in Appendix A.

3.2.2 Γ-Type Matching Network

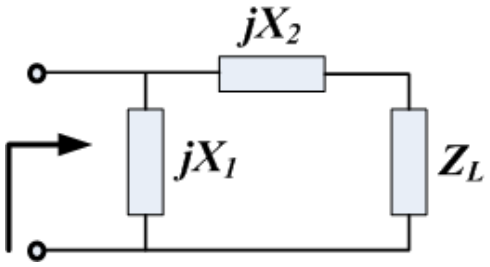


Fig. 3.2: Γ-Type matching network

The input impedance of Γ-type matching network is written as

$$\tilde{Z}_{in} = \frac{-X_L X_1 + jR_L X_1 - X_1 X_2}{R_L + j(X_L + X_1) + jX_2} \tag{3.2}$$

The input resistance and reactance are given by (3.3) and (3.4), respectively.

$$\tilde{R}_{in} = \frac{R_L X_1^2}{R_L^2 + (X_L + X_1 + X_2)^2} \tag{3.3}$$

$$\tilde{X}_{in} = X_1 - \frac{X_1^2 (X_L + X_1 + X_2)}{R_L^2 + (X_L + X_1 + X_2)^2} \tag{3.4}$$

3.2.2.1 Impact of Tunable X_2 on the Input Impedance

If Z_L and X_1 are given, the equation (3.2) can be viewed as a linear fractional transformation. Therefore, the image of X_2 under (3.2) is a circle, which is written as

$$\left| \tilde{Z}_{in} - Z_o \right|^2 = r^2 \tag{3.5}$$

According to the Appendix A, the central point and radius are calculated by

$$\left| \tilde{Z}_{in} - \left(\frac{X_1^2}{2 \cdot R_L} + jX_1 \right) \right|^2 = \left(\frac{X_1^2}{2 \cdot R_L} \right)^2 \tag{3.6}$$

The partial derivative of (3.3) with respect to X_2 is written as

$$\frac{\partial \tilde{R}_{in}}{\partial X_2} = \frac{-2R_L X_1^2 (X_L + X_1 + X_2)}{\left[R_L^2 + (X_L + X_1 + X_2)^2 \right]^2} \tag{3.7}$$

Using equation (3.4) yields the expression

$$\begin{cases} \tilde{X}_{in} > X_1 & X_L + X_1 + X_2 < 0 \\ \tilde{X}_{in} < X_1 & X_L + X_1 + X_2 > 0 \end{cases} \tag{3.8}$$

Substituting (3.8) into (3.7) yields (3.9). As shown in Fig.3.3, the input impedance point moves in a clockwise direction around the circle with the increase of X_2.

$$\tilde{X}_{in} > X_1 \quad \frac{\partial \tilde{R}_{in}}{\partial X_2} > 0 \tag{3.9-a}$$

$$\tilde{X}_{in} < X_1 \quad \frac{\partial \tilde{R}_{in}}{\partial X_2} < 0 \tag{3.9-b}$$

According to (3.10), if X_2 approaches the positive or negative infinity, the input impedance point approaches a point (0, X_1). In other words, the input impedance point cannot pass through the point (0, X_1).

$$\lim_{X_2 \to \pm\infty} \tilde{Z}_{in} = jX_1 \tag{3.10}$$

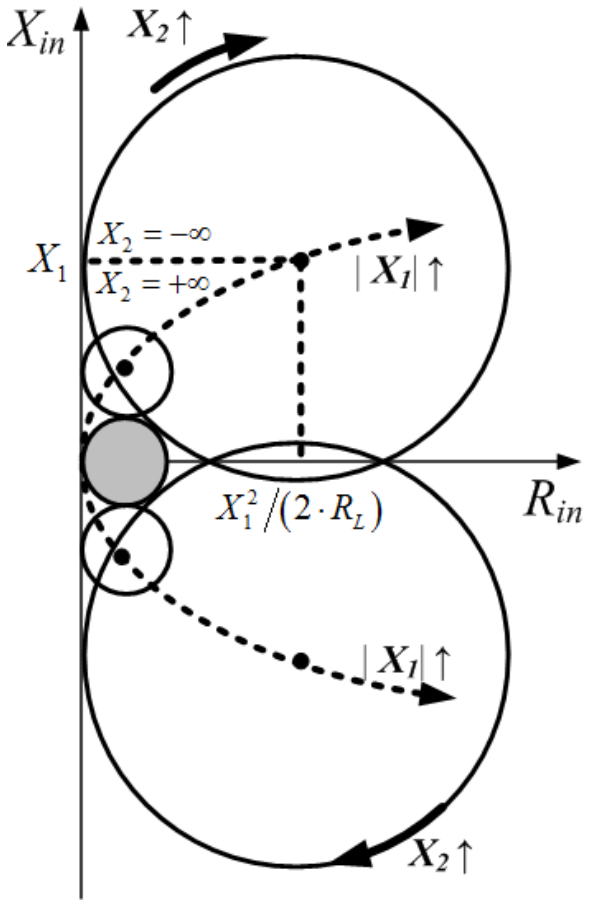


Fig. 3.3: Trajectory of Z_{in} with fixed Z_L and X_1

The trajectory of input impedance point is depicted in Fig.3.3. The circle is fully determined by Z_L and X_1. All circles are tangent to the reactance-axis. The central point moves along the dashed parabola with the increase of X_1. The input impedance point starts from a point (0, X_1), moves in a clockwise direction around the circle, and then goes back to the starting point (0, X_1) with the increase of X_2. The forbidden region is determined by the envelope of all circles.

3.2.2.2 Impact of Tunable X_1 on the Input Impedance

If Z_L and X_2 are given, the central point and radius are calculated by

$$\left|\tilde{Z}_{in} - \left(\frac{R_L^2 + (X_L + X_2)^2}{2 \cdot R_L}\right)\right|^2 = \left(\frac{R_L^2 + (X_L + X_2)^2}{2 \cdot R_L}\right)^2 \tag{3.11}$$

If X_1 approaches zero, the input impedance point approaches a point (0, 0). Moreover, the input impedance point cannot pass through the point (0, 0) because X_1 is either capacitive/negative or inductive/positive. Additionally, if X_1 approaches the positive or negative infinity, the input impedance point approaches a point (R_L, X_L+X_2).

$$\lim_{X_1 \to 0} \tilde{Z}_{in} = 0 \tag{3.12}$$

$$\lim_{X_1 \to \pm\infty} \tilde{R}_{in} = R_L \tag{3.13}$$

$$\lim_{X_1 \to \pm\infty} \tilde{X}_{in} = X_L + X_2 \tag{3.14}$$

The trajectory of input impedance point is depicted in Fig.3.4. The circle is fully determined by Z_L and X_2. All circles are tangent to the reactance-axis. The central point moves along the resistance-axis with the increase of X_2. The forbidden region is determined by R_L. The input impedance point starts from a point (R_L, X_L+X_2), moves in a clockwise direction around the circle, and then goes back to the starting point (R_L, X_L+X_2) with the increase of X_1. The input impedance point cannot be located in the forbidden region.

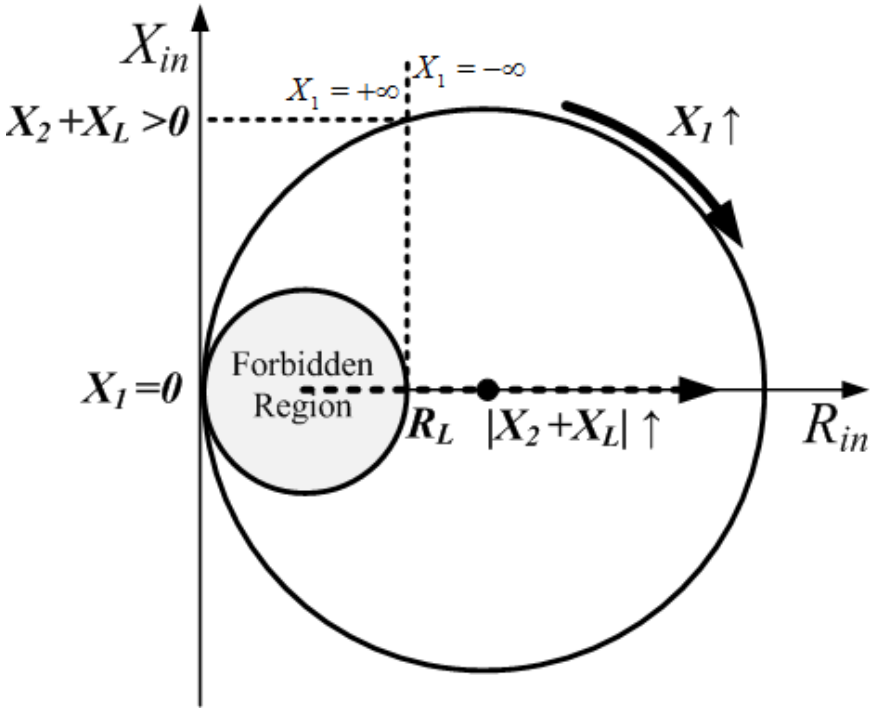


Fig. 3.4: Trajectory of Z_{in} with fixed Z_L and X_2

3.3 Objective Function: S_{11} Parameter

First, we will introduce some related concepts and definitions.

- **Local Minimum:** A local minimum of a function is a point where the function value is smaller than at nearby points, but possibly greater than at a distant point.
- **Global Minimum:** A global minimum is a point where the function value is smaller than at all other feasible points. If you need a global optimum, you must find an initial value for your solver in the basin of attraction of a global optimum.
- **Unimodal Function:** A function $f : R^n \mapsto R$ is called quasiconvex (or unimodal) if its domain and all its sublevel sets $S_\alpha = \{x \in domf | f(x) \leq \alpha)\}$ are convex. [Boyd, Vandenberghe, Convex Optimization, Page 95]

In practice, the S_{11} parameter is used to evaluate the return loss of tunable matching network. The optimization problem is formulated as (3.15). According to this formula, for any load impedance $Z_L = R_L + jX_L$, there exists a set of parameters $\{X_1^*, X_2^*, X_3^*\}$ in the feasible region which ensures the minimum value of S_{11} parameter is zero. In addition, the optimum point $\{X_1^*, X_2^*, X_3^*\}$ should be converged from any starting point $\{X_1^0, X_2^0, X_3^0\}$ in the feasible region.

To achieve these two objectives, the design strategies of different tunable matching networks in section 3.4.2, 3.4.4, 3.4.6 guarantee the existence of optimal point $\{X_1^*, X_2^*, X_3^*\}$, the convergence criteria of different tunable matching networks in section 3.4.1, 3.4.3, 3.4.5 guarantee the the probability of of finding the optimal point $\{X_1^*, X_2^*, X_3^*\}$ is high.

$$\begin{cases} min & S_{11}(X_1, X_2, X_3) = \left| \frac{R_{in}+jX_{in}-50}{R_{in}+jX_{in}+50} \right| \\ where & R_{in} = \frac{R_L X_1^2}{R_L^2+(X_L+X_1+X_2)^2} \\ & X_{in} = X_1 + X_3 - \frac{X_1^2(X_L+X_1+X_2)}{R_L^2+(X_L+X_1+X_2)^2} \\ & R_{Lmin} \le R_L \le R_{Lmax} \\ & X_{Lmin} \le X_L \le R_{Xmax} \\ s.t: & X_{1min} \le X_1 \le X_{1max} \\ & X_{2min} \le X_2 \le X_{2max} \\ & X_{3min} \le X_3 \le X_{3max} \end{cases} \tag{3.15}$$

The reflection coefficient (3.16) is a typical linear fractional transformation. The inverse transformation of (3.16) is written as (3.17). Hence, a circle in the Γ-plane is mapped to either a circle or a line in the z-plane.

$$\Gamma = \frac{Z_{in} - 50}{Z_{in} + 50} \tag{3.16}$$

$$Z_{in} = 50 \times \frac{1+\Gamma}{1-\Gamma} \tag{3.17}$$

As shown in Fig.3.5, the solid circles (3.18) in the Γ-plane are mapped into the solid circles (3.19) in the z-plane.

$$\left(\mathrm{Re}\left(\Gamma\right)\right)^2 + \left(\mathrm{Im}\left(\Gamma\right)\right)^2 = C \quad 1 > C \ge 0 \tag{3.18}$$

$$\left(\mathrm{Re}\left(Z_{in}\right) - 50 \times \frac{1+C^2}{1-C^2}\right)^2 + \left(\mathrm{Im}\left(Z_{in}\right)\right)^2 = \left(50 \times \frac{2C}{1-C^2}\right)^2 \tag{3.19}$$

Additionally, the unit circle (3.20) in the Γ-plane is mapped into the dashed line in the z-plane.

$$\left|\frac{Z_{in}-50}{Z_{in}+50}\right|=1 \tag{3.20}$$

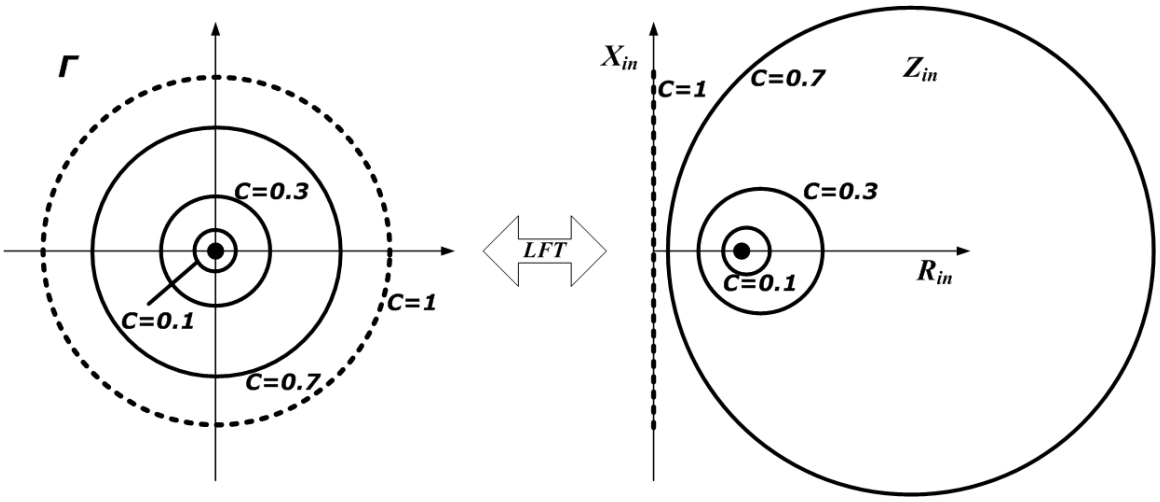


Fig. 3.5: The relationship between Γ-plane and z-plane

Apparently, the S_{11} is a unimodal function of Z_{in}. A proof is as follows: the sublevel sets are defined as $S_C = \{Z_{in} \in domS_{11} | S_{11} \leq C)\}$. For any $C < 1$, the corresponding sublevel set S_C is written as (3.19). Because the sphere is a convex set, the S_{11} is a quasiconvex (or unimodal) function of Z_{in} according to the definition.

3.4 Convergence Criteria of T-type Network

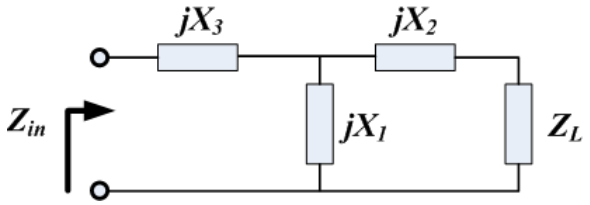


Fig. 3.6: T-type matching network

To reduce the forbidden region and improve the Q-factor of matching network, the T-type matching network is shown in Fig.3.6. The input impedance of T-type matching network is written as

$$Z_{in} = \tilde{Z}_{in} + jX_3 \tag{3.21}$$

The first term on the right-hand side of (3.21) is the input impedance of Γ-type matching network. The X_3 is used to slide the circle in Fig.3.3 and Fig.3.4 along the reactance-axis.

3.4.1 TMN with Fixed X_1

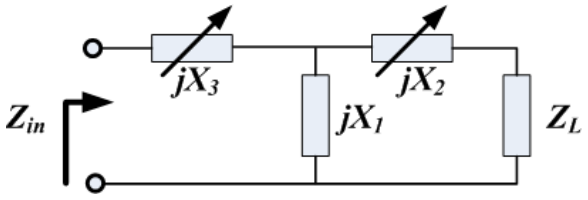


Fig. 3.7: Tunable matching network with fixed reactance X_1

Assume that X_1 is an inductor and X_3 is a capacitor. As shown in Fig.3.8, the solid circle is fully determined by X_1 and Z_L. Firstly, the input impedance point of Γ-type network is moved along the solid circle by X_2 from the point *A* to the point *B*. Subsequently, the X_3 slides the curve *AB* from A_1B_1 to A_2B_2. Finally, the tunable area $A_1B_1B_2A_2$ is specified. The S_{11} value of this tunable area is given by the left-side of Fig.3.8.

If the curve *AB* is on the top-half or lower-half of the circle, any impedance point in the tunable area $A_1B_1B_2A_2$ is obtained by a unique set of tuning parameters (X_2, X_3). In addition, the curve *CDE* is divided into two parts, upper-half curve *CD* and lower-half curve *DE*. Similarly, the tunable areas generated by curve *CD* and *DE* are area $C_1D_1D_2C_2$ and $D_1E_1E_2D_2$, respectively. However, these two tunable areas overlap each other. Any impedance point in the overlapping area D_1FD_2 can be obtained by two different sets of parameters (X_2, X_3). As a result, the combination of two tunable regions ($C_1D_1D_2C_2$ and $D_1E_1E_2D_2$) could result in a multimodal function.

In a word, as long as the X_2 slides the impedance point along the upper-half or lower-half of the circle, we are most likely to converge to the optimum point. In accordance with section 3.2, the input impedance point cannot pass through the point (0, X_1). Therefore, the convergence criterion (3.22) guarantees that the impedance point controlled by X_2 cannot pass through the point *D*. More detailed discussions are clarified in the Appendix D.

$$\left[\mathrm{Im}\left(\tilde{Z}_{in}\left(\max X_2\right)\right) - X_1\right] \cdot \left[\mathrm{Im}\left(\tilde{Z}_{in}\left(\min X_2\right)\right) - X_1\right] \geq 0 \tag{3.22}$$

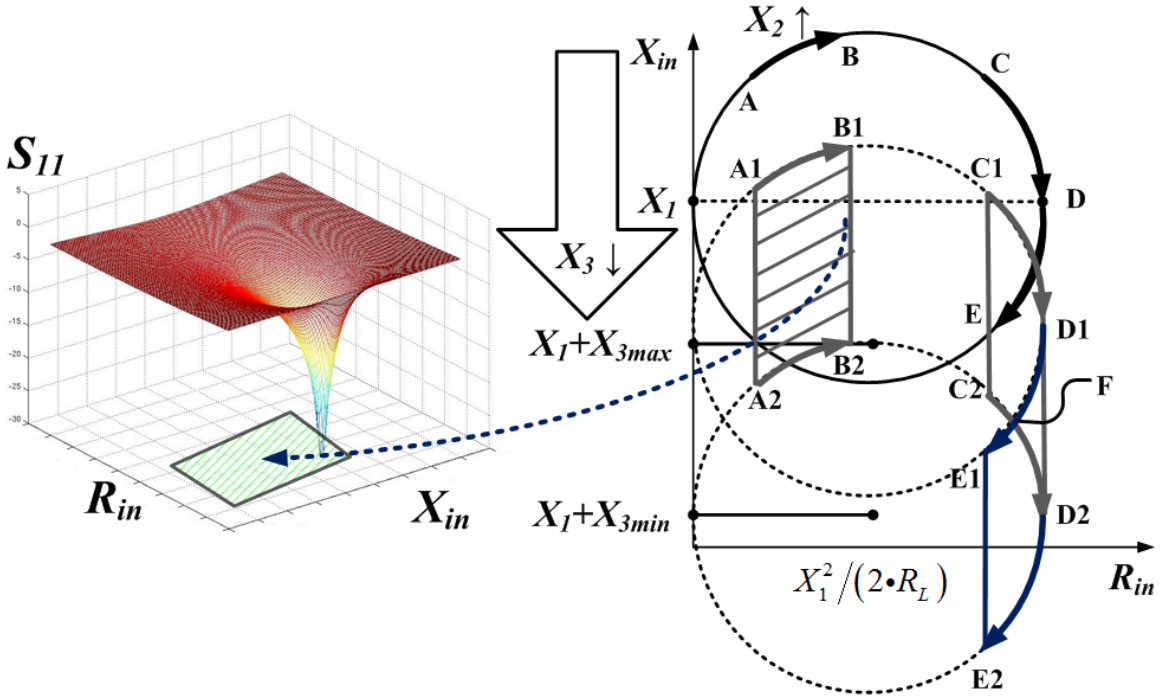


Fig. 3.8: Convergence criteria of TMN with fixed reactance X_1

3.4.2 Design Strategy

By applying the convergence criterion (3.22), design strategy of tunable matching network with fixed X_1 is proposed. Because the tunable T-type matching network is lossless, the source impedance matching and load impedance matching are achieved simultaneously.

$$Z_{in} = R_s^* \quad \Leftrightarrow \quad Z_{out} = Z_L^* \tag{3.23}$$

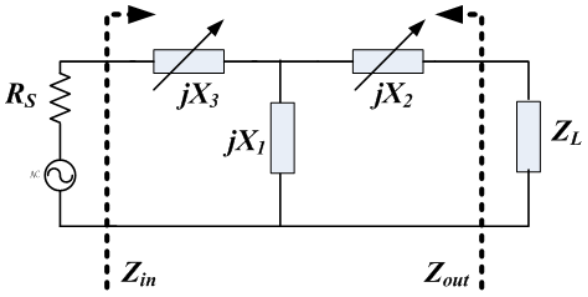


Fig. 3.9: Source matching and load matching

This section designs a tunable matching network from the source side since the load impedance is a variable. Therefore, the output impedance of the tunable matching network should be equal to the complex conjugate of the load impedance. As shown in

Fig.3.10, the solid circle is fully determined by R_S and X_1. The X_3 slides the impedance point from X_{3-1} to X_{3-2}. Subsequently, the X_2 slides the curve $X_{3-1}X_{3-2}$ along the reactance-axis. Once the matching region marked by bold line is capable of covering the area of complex conjugate of load impedance, the load impedance variation can be perfectly calibrated by this tunable matching network. Therefore, this section designs the tunable matching network as follows:

Step 1: Choose X_1 according to (3.24). The X_3 is determined by (3.25). Additionally, the X_2 can be determined by covering the area of complex conjugate of the load impedance.

$$\frac{X_1^2}{R_S} \geq R_{L\max} \tag{3.24}$$

$$X_{3\_1,4} + X_1 + X_s = \pm\sqrt{\frac{R_s X_1^2}{R_{L\min}} - R_s^2} \tag{3.25-a}$$

$$X_{3\_2,3} + X_1 + X_s = \pm\sqrt{\frac{R_s X_1^2}{R_{L\max}} - R_s^2} \tag{3.25-b}$$

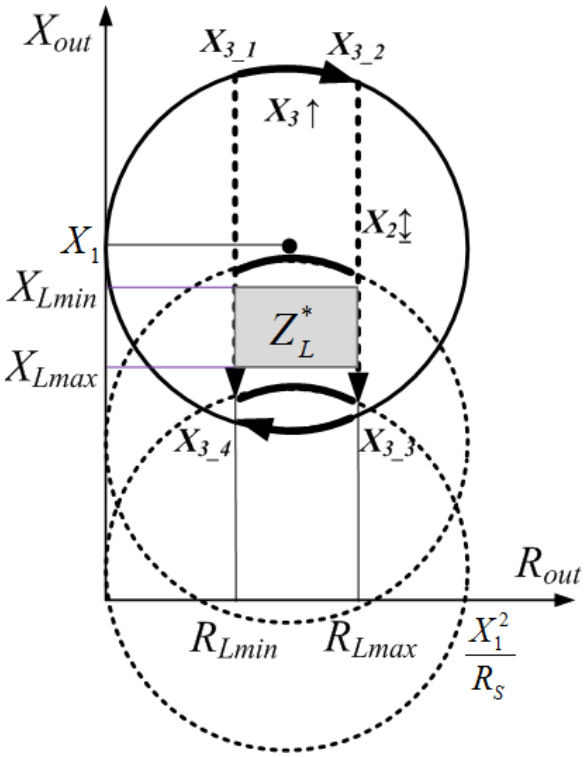


Fig. 3.10: Design strategy of tunable T-type network with fixed X_1

Step 2: Check convergence criterion (3.22). By simplifying (3.22), the criterion is rewritten as (3.27). The feasible region of X_L is depicted in Fig.3.11.

$$[X_L + X_{2\max} + X_1] \cdot [X_L + X_{2\min} + X_1] \geq 0 \tag{3.26}$$

$$X_{L\min} > -(X_{2\min} + X_1) \tag{3.27-a}$$

$$X_{L\max} < -(X_{2\max} + X_1) \tag{3.27-b}$$

Step 3: Check the Q-factor of tunable matching network. If the Q-factor does not meet the specification, update X_1 according to (3.24) and repeat the design flow until all constraints are met. In the end of this subsection, it is worth to mention that the X_2 and X_3 are mainly responsible for covering the area of complex conjugate of the load impedance. The X_1 is mainly responsible for improving the Q-factor of the matching network.

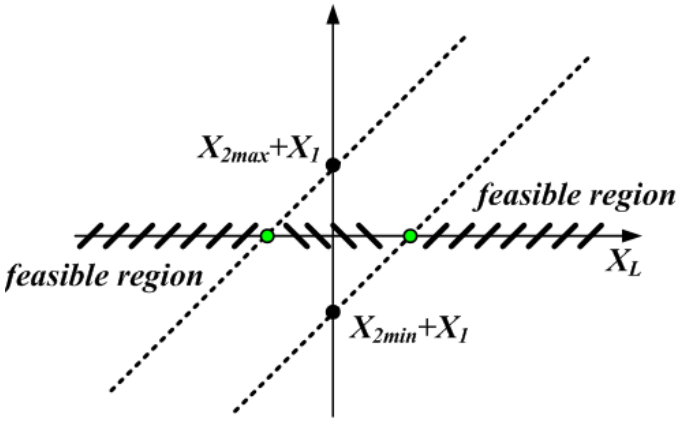


Fig. 3.11: The feasible region of X_L

3.4.3 TMN with Fixed X_2

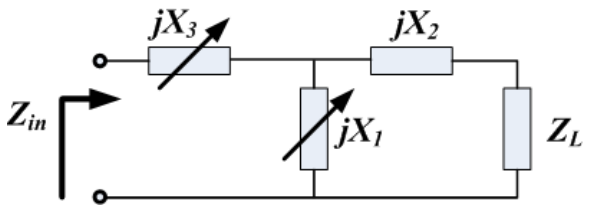


Fig. 3.12: Tunable T-type matching network with fixed X_2

As shown in Fig.3.13, the solid circle is fully determined by X_2 and Z_L. Assume that X_3 is a capacitor. Firstly, the input impedance point of Γ-type network is moved by X_1 from point *A* to point *B*. Subsequently, the X_3 slides the curve *AB* from A_1B_1 to A_2B_2. Finally, the tunable area $A_1B_1B_2A_2$ is specified. The S_{11} value of this tunable area is given by the left-side of Fig.3.13.

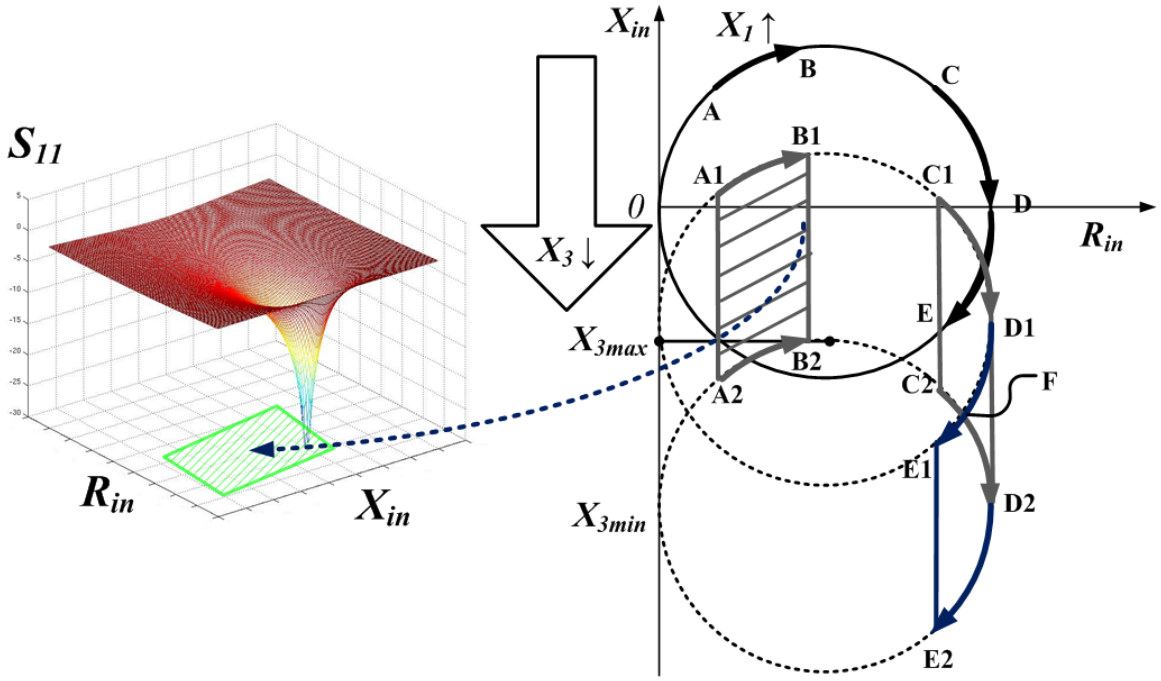


Fig. 3.13: Convergence criteria of TMN with fixed reactance X_2

As discussed in section 3.4.1, as long as the X_1 slides the impedance point along the upper-half or lower-half of the circle, the objective function is converged. In accordance with section 3.2, the input impedance point of Γ-type matching network cannot pass through the point (0, 0). Therefore, the criterion (3.28) guarantees that the impedance point controlled by X_1 cannot pass through the point *D*.

$$\left[\mathrm{Im}\left(\tilde{Z}_{in}\left(\max X_1\right)\right)\right] \cdot \left[\mathrm{Im}\left(\tilde{Z}_{in}\left(\min X_1\right)\right)\right] \geq 0 \tag{3.28}$$

3.4.4 Design Strategy

Similarly, this section designs the tunable matching network from the source side since the load impedance is a variable.

Step 1: Choose X_2. As shown in Fig.3.14, the tunable region is determined by X_1 and X_3. The forbidden region is determined by R_S. The X_2 slides the matching region into the tunable region. The forbidden region is not allowed to overlap with the matching region. Hence, a simple and effective algorithm that is able to detect the intersection between a rectangle and a circle is highly desired [17], which will be discussed in section 3.9.

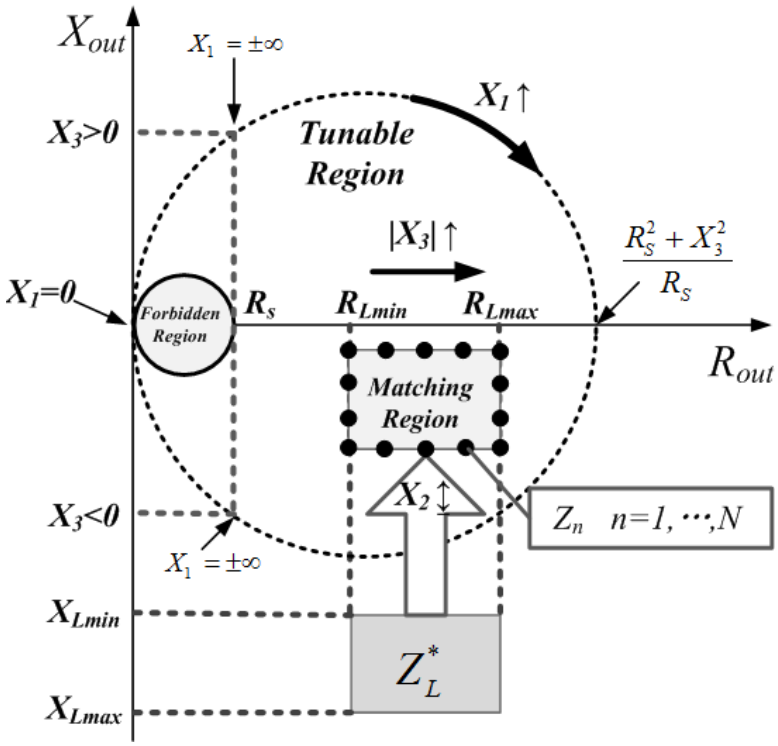


Fig. 3.14: Design of tunable T-type network with fixed X_2

Step 2: We utilize a set of impedance points Z_n located on the boundary of matching region to calculate the range of X_1 and X_3. As shown in Fig.3.15, the central point of the circle is fully determined by X_3. Therefore, the X_{3n} for each impedance point Z_n is calculated by

$$\left(\frac{R_s^2+X_{3n}^2}{2R_s}\right)^2 = \left(R_n - \frac{R_s^2+X_{3n}^2}{2R_s}\right)^2 + X_n^2 \tag{3.29}$$

The solution of (3.29) is

$$X_{3n}^2 = \frac{R_s}{R_n}\left(X_n^2+R_n^2 - R_nR_s\right) \tag{3.30}$$

If X_{3n} is given, the X_{1n} for each impedance point Z_n should satisfy the following two equations. Furthermore, the range of X_1 and X_3 can be estimated by the maximum and minimum value of X_{1n} and X_{3n}, respectively.

$$R_n = \frac{R_sX_{1n}^2}{R_s^2+(X_{1n}+X_{3n})^2} \tag{3.31-a}$$

$$X_n = X_{1n} - \frac{X_{1n}^2\cdot(X_{1n}+X_{3n})}{R_s^2+(X_{1n}+X_{3n})^2} \tag{3.31-b}$$

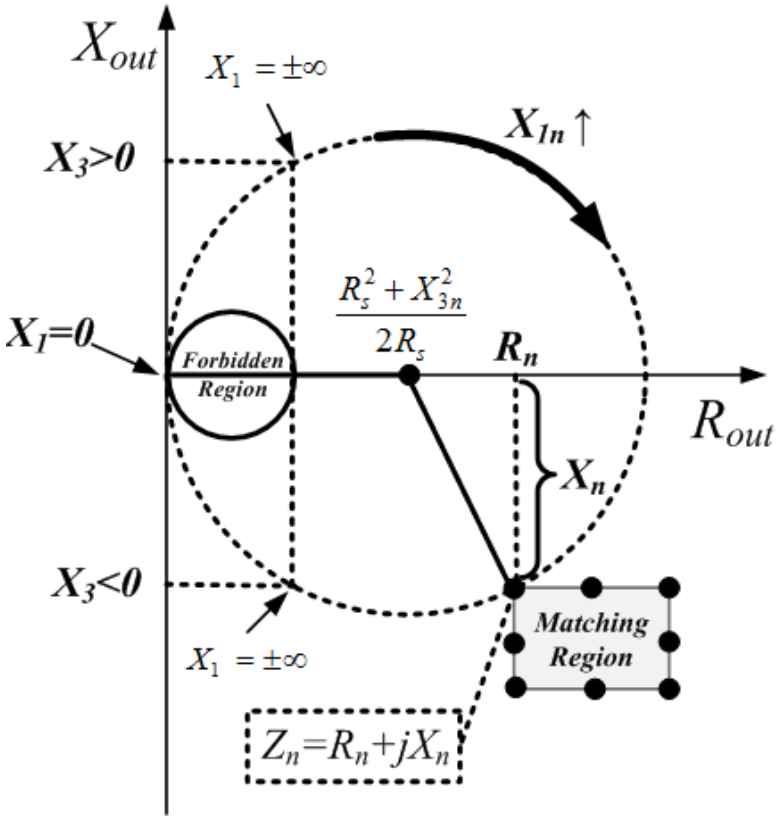


Fig. 3.15: The calculation of X_{2n} and X_{3n}

Step 3: Check convergence criterion (3.28). By simplifying (3.28), the criterion is written as

$$\left[X_{1\,\min} - \frac{X_{1\,\min}^2\left(X_L + X_{1\,\min} + X_2\right)}{R_L^2 + \left(X_L + X_{1\,\min} + X_2\right)^2}\right] \cdot \left[X_{1\,\max} - \frac{X_{1\,\max}^2\left(X_L + X_{1\,\max} + X_2\right)}{R_L^2 + \left(X_L + X_{1\,\max} + X_2\right)^2}\right] \geq 0 \quad (3.32)$$

Step 4: Check the Q-factor of tunable matching network. If the Q-factor does not meet the specifications, update X_2 and repeat the design flow until all constraints are met. In the end of this subsection, it is worth to mention that the X_1 and X_3 are mainly responsible for covering the area of complex conjugate of the load impedance. The X_2 is mainly responsible for improving the Q-factor of the matching network.

3.4.5 TMN with Fixed X_3

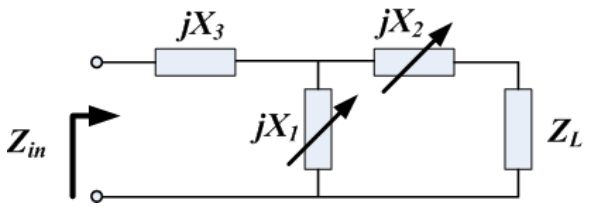


Fig. 3.16: Tunable T-type matching network with fixed X_3

As shown in Fig.3.17, all circles determined by X_2 are tangent to the reactance axis and have a common impedance point (0, X_3). In accordance with section 3.2, the input impedance point cannot pass through the point (0, X_3). In addition, the X_{2a} and X_{2b} defined by (3.33) result in a same circle.

$$\begin{cases} X_{2a} = -X_L + \Delta \\ X_{2b} = -X_L - \Delta \end{cases} \quad \Delta \geq 0 \tag{3.33}$$

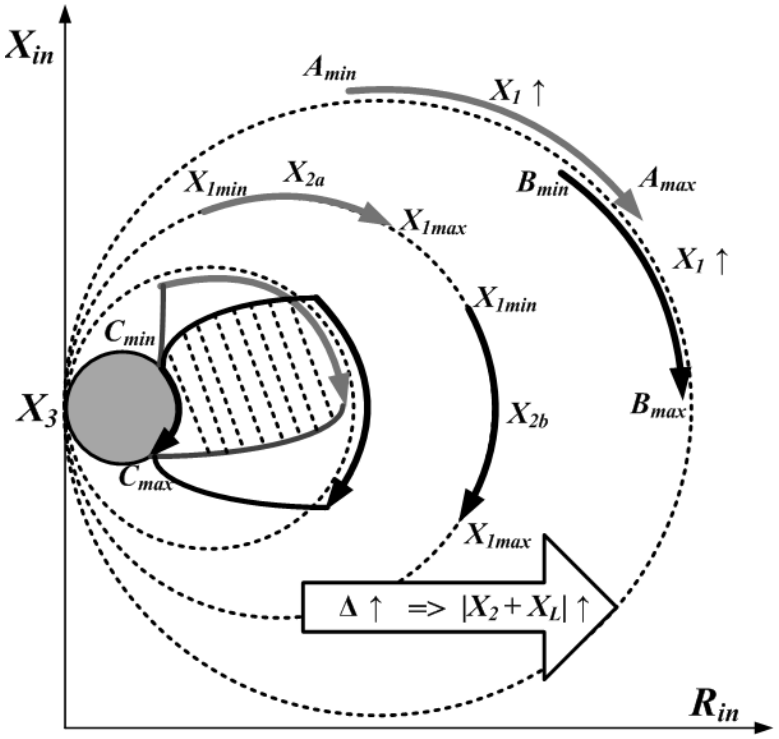


Fig. 3.17: Convergence criteria of TMN with fixed reactance X_3

As shown in Fig.3.17, if X_2 is equal to -X_L, the input impedance point is moved by X_1 from C_{min} to C_{max} along the minimum circle. By increasing or decreasing X_2 with the same variation Δ, the input impedance point is moved along the same bigger circle.

Assume that the impedance point moves along the curve $A_{min}A_{max}$ with X_{2a} and along the curve $B_{min}B_{max}$ with X_{2b}. By increasing Δ from zero to positive infinity, the curve $A_{min}A_{max}$ and curve $B_{min}B_{max}$ separate from the curve $C_{min}C_{max}$, and then converge together, which leads to an overlapping area. Similarly, the combination of two tunable regions ($C_{min}C_{max}A_{min}A_{max}$ and $C_{min}C_{max}B_{min}B_{max}$) could result in a multimodal function. The convergence criterion is written as

$$-X_L \notin \left[\begin{array}{cc} X_{2\,\min} & X_{2\,\max} \end{array} \right] \tag{3.34}$$

Substituting (3.33) to (3.2) yields

$$\tilde{Z}_{in}\left(X_{1a}\right) = \frac{-X_L X_{1a} + jR_L X_{1a} - X_{1a}\left(-X_L + \Delta\right)}{R_L + j(X_L + X_{1a}) + j\left(-X_L + \Delta\right)} \tag{3.35-a}$$

$$\tilde{Z}_{in}\left(X_{1b}\right) = \frac{-X_L X_{1b} + jR_L X_{1b} - X_{1b}\left(-X_L - \Delta\right)}{R_L + j(X_L + X_{1b}) + j\left(-X_L - \Delta\right)} \tag{3.35-b}$$

If curve $A_{min}A_{max}$ and curve $B_{min}B_{max}$ overlap each other, X_{1a} and X_{1b} should satisfy (3.36). By simplifying (3.36), the relationship between X_{1a} and X_{1b} is illustrated by (3.37).

$$\tilde{Z}_{in}\left(X_{1a}\right) = \tilde{Z}_{in}\left(X_{1b}\right) \tag{3.36}$$

$$X_{1a}\left(X_{1b}, \Delta\right) = \frac{(R_L^2 + \Delta^2) \cdot X_{1b}}{R_L^2 + \Delta^2 - 2 \cdot \Delta \cdot X_{1b}} \tag{3.37}$$

Furthermore, the distance between X_{1a} and X_{1b} is written as

$$d = X_{1a} - X_{1b} = \frac{2 \cdot \Delta \cdot X_{1b}^2}{R_L^2 + \Delta^2 - 2 \cdot \Delta \cdot X_{1b}} \tag{3.38}$$

The equation (3.39) and (3.40) demonstrate that the distance is increased from zero to the maximum value by increasing Δ from zero to R_L; the distance is decreased from the maximum value to zero by increasing Δ from R_L to the positive infinity.

$$\frac{\partial d}{\partial \Delta} \propto R_L^2 - \Delta^2 \tag{3.39}$$

$$\lim_{\Delta \to \infty} d = \lim_{\Delta \to 0} d = 0 \tag{3.40}$$

3.4.6 Design Strategy

Similarly, this subsection designs the tunable matching network from the source side since the load impedance is a variable. The solid circle in Fig.3.18 is determined by R_S

and X_3. The X_1 slides the impedance point from X_{1-3} to X_{1-4}. Subsequently, the X_2 slides the curve $X_{1-3}X_{1-4}$ along the reactance axis. Once the tunable area is capable of covering the area of complex conjugate of load impedance, the load impedance variation is perfectly calibrated.

Step 1: Choose X_3 according to (3.41). The X_1 is calculated by (3.42). Additionally, the X_2 is determined by covering the area of complex conjugate of the load impedance.

$$\frac{R_s^2 + X_3^2}{R_S} \geq R_{L\max} \tag{3.41}$$

$$X_{1\_1,4} = \frac{-2R_{L\min}X_3 \pm \sqrt{\left(2R_{L\min}X_3\right)^2 - 4R_{L\min}\left(R_{L\min} - R_S\right)\left(R_s^2 + X_3^2\right)}}{2 \times \left(R_{L\min} - R_S\right)} \tag{3.42-a}$$

$$X_{1\_2,3} = \frac{-2R_{L\max}X_3 \pm \sqrt{\left(2R_{L\max}X_3\right)^2 - 4R_{L\max}\left(R_{L\max} - R_S\right)\left(R_s^2 + X_3^2\right)}}{2 \times \left(R_{L\max} - R_S\right)} \tag{3.42-b}$$

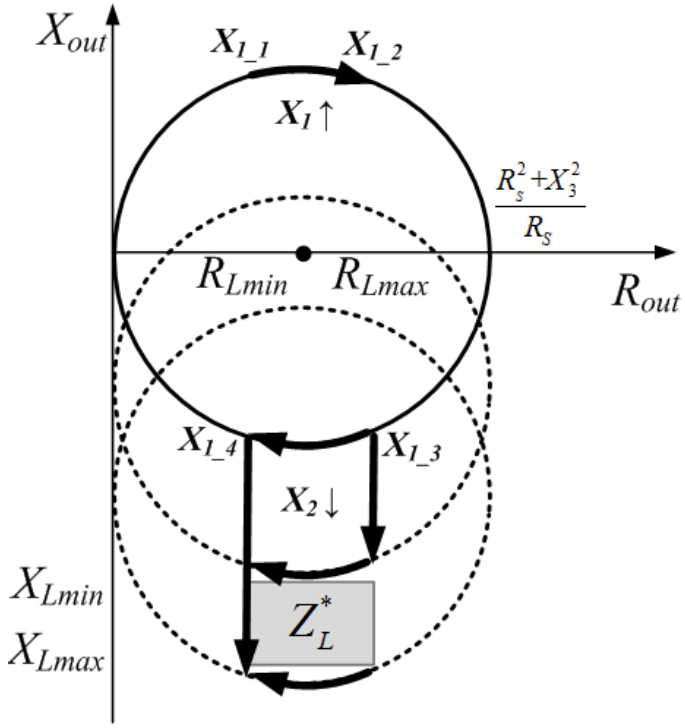


Fig. 3.18: Design of tunable T-type network with fixed X_3

Step 2: Check convergence criterion (3.43).

$$-X_L \notin \left[\begin{array}{cc} X_{2\min} & X_{2\max} \end{array} \right] \tag{3.43}$$

Step 3: Check the Q-factor of tunable matching network. If the Q-factor does not meet the specification, update X_3 according to (3.41), and then repeat the design flow until all constraints are met. It is worth to mention that the X_1 and X_2 are mainly responsible for covering the area of complex conjugate of the load impedance. The X_3 is mainly responsible for improving the Q-factor of the matching network.

3.4.7 Tunable X_1, X_2, and X_3

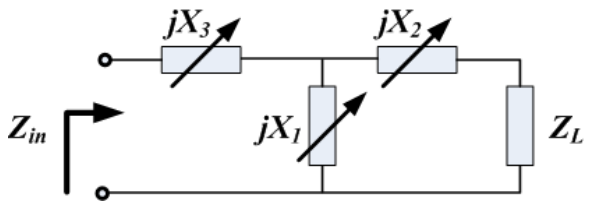


Fig. 3.19: Tunable T-type network with tunable components X_1, X_2, and X_3

In case of the tunable X_1, X_2, and X_3, the tunable region in Fig.3.20 is moved along the reactance axis by X_3. In case of the fixed X_1 and X_2, the objective function S_{11} is a unimodal function of tunable X_3. Therefore, the convergence criterion is written as

(1) Set X_1 to be (X_{1min}+X_{1max})/2. Set X_2 to be (X_{2min}+X_{2max})/2. Calibrate X_3 to reach the minimum S_{11}.

(2) In case the convergence criterion (3.34) is satisfied, the global optimum point can be reached by tuning X_1 and X_2.

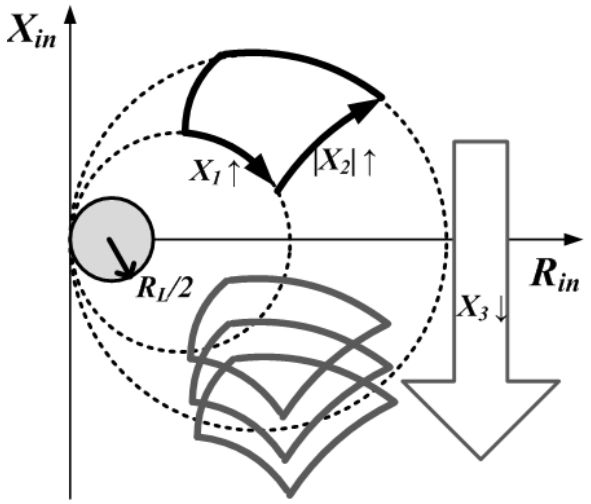


Fig. 3.20: X_1, X_2, and X_3 are variables

3.5 Convergence Criteria of Π-type Network

In addition to the T-type matching network, the Π-Type matching network is also widely used.

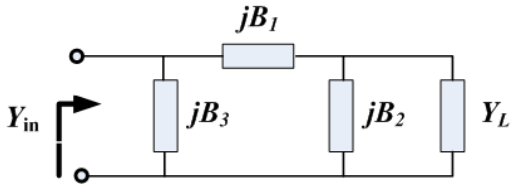


Fig. 3.21: Π-type matching network

As shown in Fig.3.21, the input admittance of Π-type matching network is written as

$$\tilde{Y}_{in} = \frac{-B_L B_1 + jG_L B_1 - B_1 B_2}{G_L + j(B_L + B_1) + jB_2} \tag{3.44}$$

Since the equation (3.44) is identical to (3.2), all conclusions in the T-type matching network can be reused in the Π-type matching network. The equation (3.22), (3.28), and (3.34) are rewritten as (3.45), (3.46), and (3.47), respectively.

$$\left[\mathrm{Im}\left(\tilde{Y}_{in}\left(\max B_2\right)\right) - B_1\right] \cdot \left[\mathrm{Im}\left(\tilde{Y}_{in}\left(\min B_2\right)\right) - B_1\right] \geq 0 \tag{3.45}$$

$$\left[\mathrm{Im}\left(\tilde{Y}_{in}\left(\max B_1\right)\right)\right] \cdot \left[\mathrm{Im}\left(\tilde{Y}_{in}\left(\min B_1\right)\right)\right] \geq 0 \tag{3.46}$$

$$-B_L \notin \left[\begin{array}{cc} B_{2\min} & B_{2\max} \end{array}\right] \tag{3.47}$$

3.6 Adaptive Impedance Matching Algorithm

3.6.1 Single Step Algorithm

In case of matching network with two tunable components, the single step algorithm [1] can be written as Tab.3.1. The maximum number of iterations is $2^{S1-1} + 2^{S2-1}$. In this project, the digital control signals *S1* and *S2* are 8-bit. Additionally, if the convergence criteria can be satisfied, the single step algorithm is capable of reaching the neighbourhood of matching point.

Tab. 3.1: Single step algorithm

Initialization: K1 = 2^{S1-1}, K2 = 2^{S2-1}, temp = 0;
while(temp == 0)
S11-M = f(K1 ,K2);
S11-U = f(K1+1,K2);
S11-D = f(K1-1,K2);
S11-L = f(K1 ,K2-1);
S11-R = f(K1 ,K2+1);
MinS11 = min(S11-U, S11-D, S11-L, S11-R);
if (S11-M < MinS11)
temp = 1;
else
if (S11-U == MinS11) K1 = K1 + 1;
if (S11-D == MinS11) K1 = K1 - 1;
if (S11-L == MinS11) K2 = K2 - 1;
if (S11-R == MinS11) K2 = K2 + 1;
end
endwhile

3.6.2 Binary Search Algorithm

This section proposes a novel fast tuning algorithm for tunable matching network. In contrast to the single step algorithm, the convergence speed is improved from *O(N)* to *O(log(N))*.

As shown in Fig.3.8, if the convergence criteria are satisfied, the tunable X_2 is proportional to R_{in} and the tunable X_3 is proportional to X_{in} if X_2 is given. Hence, the binary search algorithm can be used to accelerate the convergence speed. The maximum number of iterations is *S2+S3*.

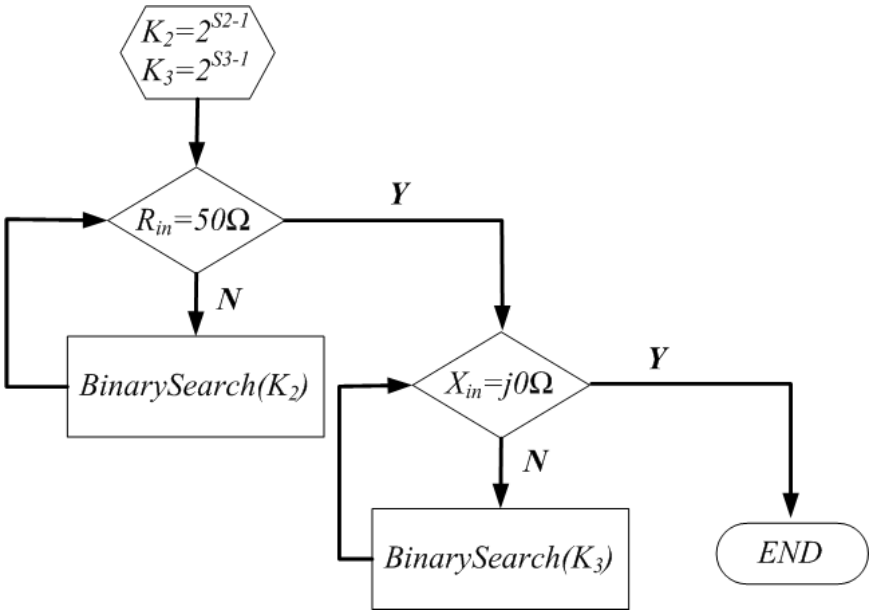


Fig. 3.22: Binary search tuning algorithm with fixed X_1

Similarly, as shown in Fig.3.13, if the convergence criteria are satisfied, the tunable X_1 is proportional to R_{in} and the tunable X_3 is proportional to X_{in} if X_1 is given. The maximum number of iterations is *S1+S3*.

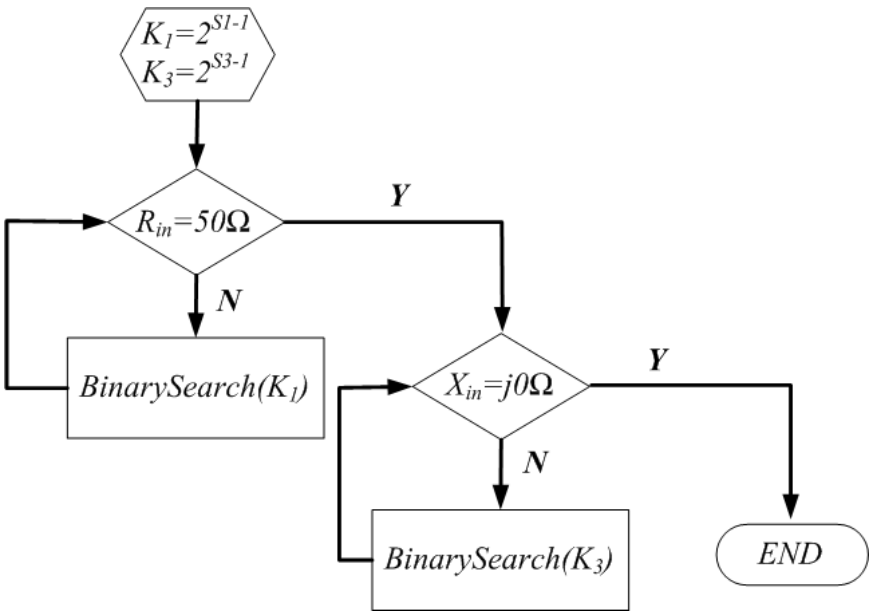


Fig. 3.23: Binary search tuning algorithm with fixed X_2

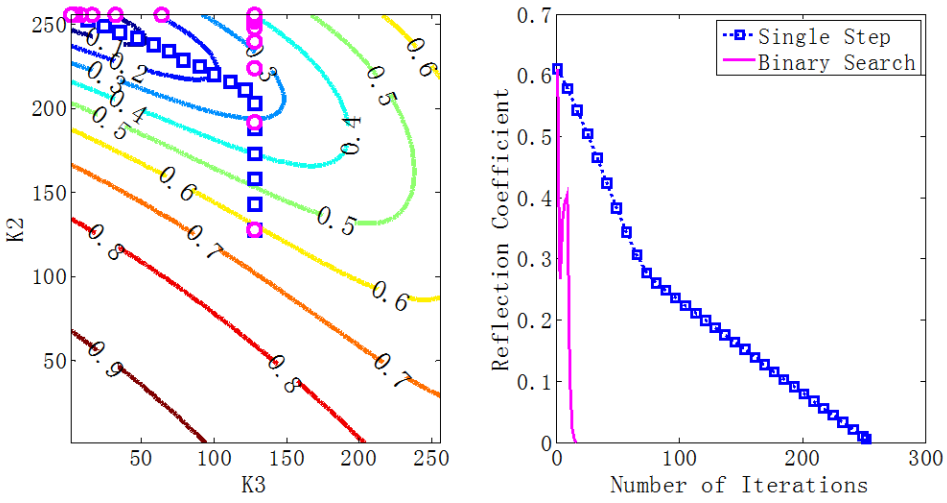
3.7 Simulation Results of Lossless Matching Networks

Antenna impedance variation has been discussed in [27,28,29]. In [30], the antenna impedance Z_L roughly lies in the range $30\Omega < R_L < 100\Omega$ and $30\Omega < X_L < 100\Omega$. The simulation results are shown in Fig.3.24, 3.25, and 3.26, respectively. The left side of each figure demonstrates that we can converge to the optimal point.

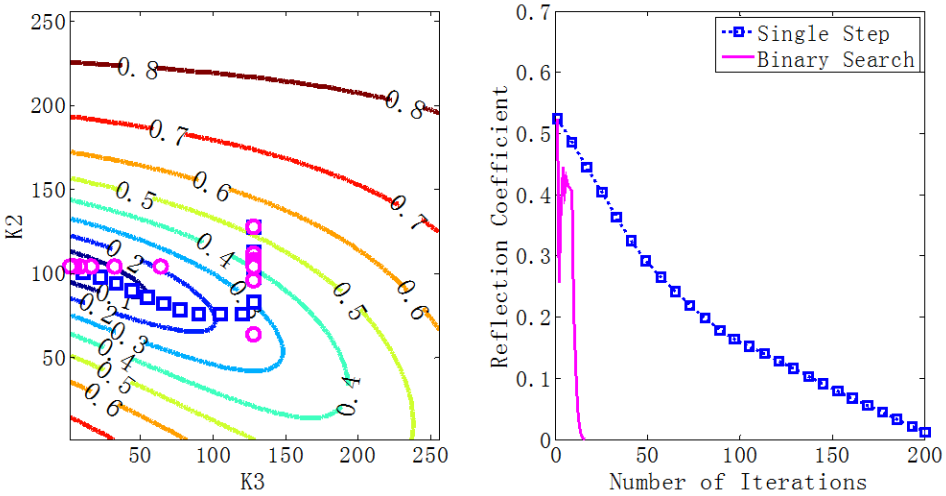
3.7.1 Simulation Results of TMN with Fixed X_1

Tab. 3.2: Tunable matching network with fixed reactance X_1

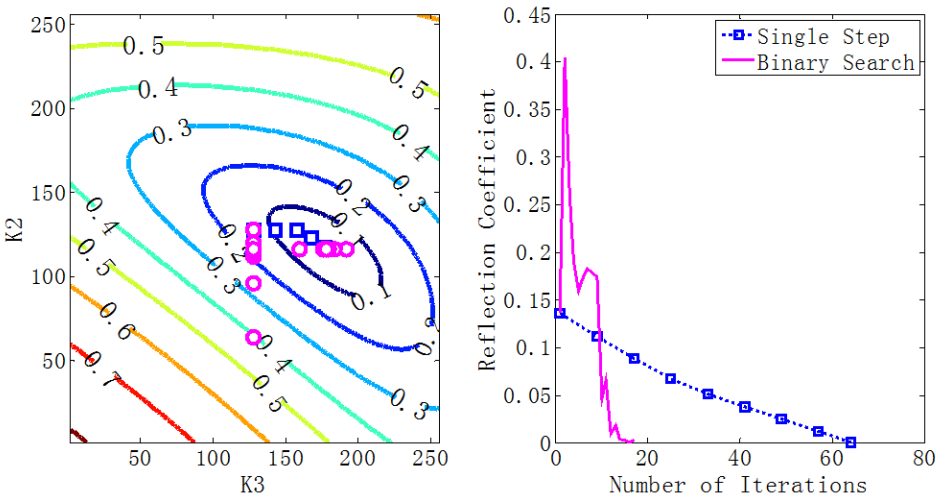
	Resistance (Ω)	Reactance (jΩ)
Source Impedance Z_S	50	0
Load Impedance Z_L	$[30, 100]$	$[0, 100]$
Fixed Inductor X_1	0	141.4
Tunable Capacitor X_2	0	$[-414.6, -246.8]$
Tunable Capacitor X_3	0	$[-317.1, -228.0]$



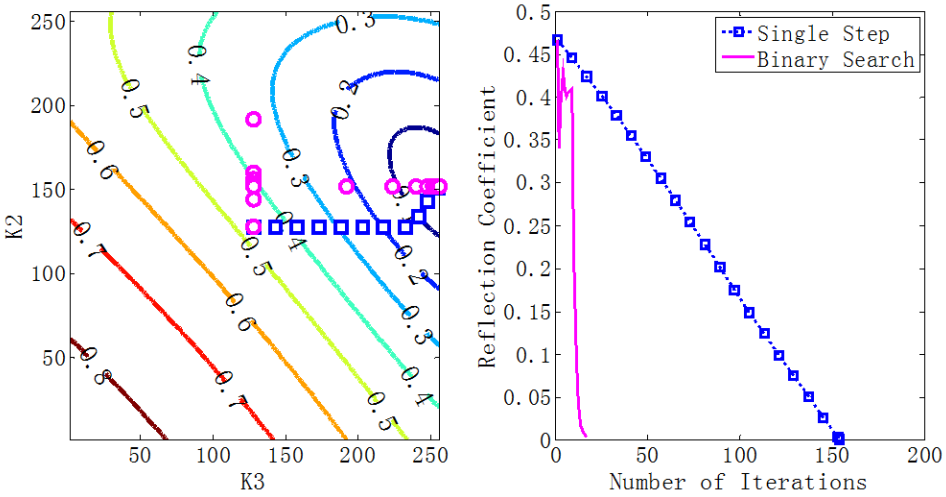
(a) Load Impedance is equal to 30 (Ω)



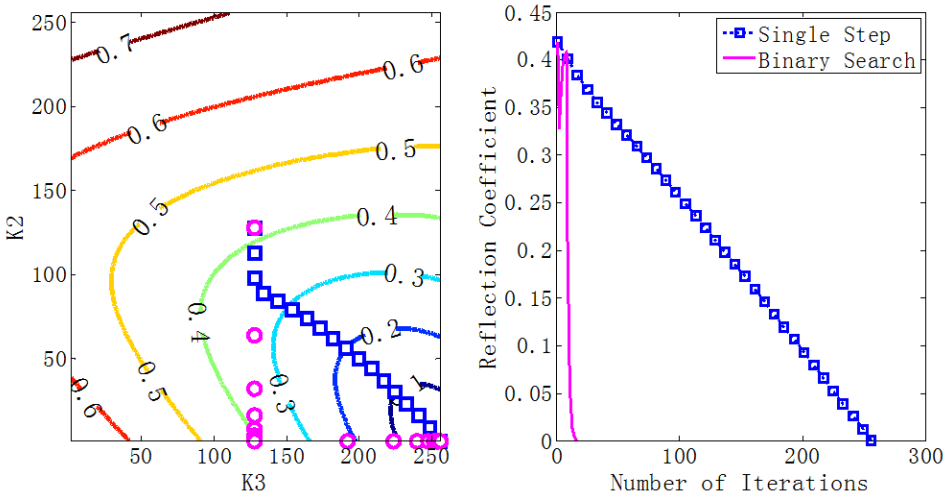
(b) Load Impedance is equal to 30+j100 (Ω)



(c) Load Impedance is equal to 65+j50 (Ω)



(d) Load Impedance is equal to 100 (Ω)



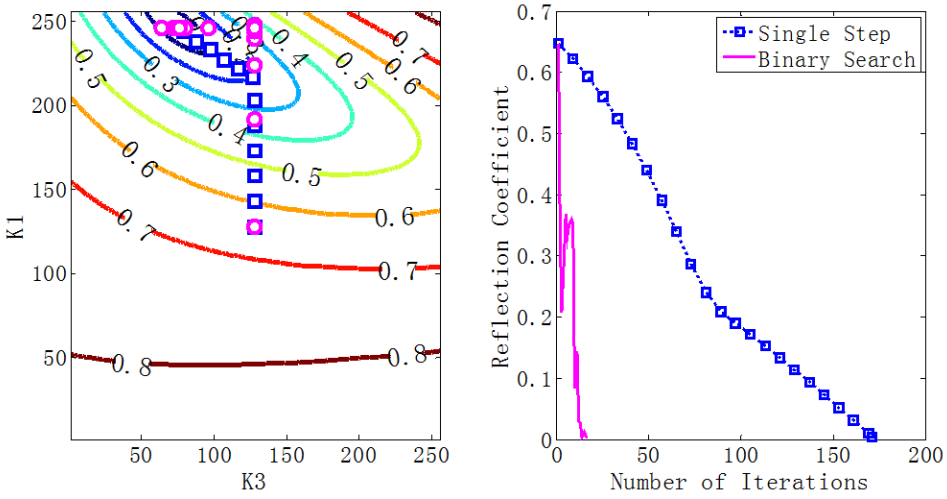
(e) Load Impedance is equal to 100+j100 (Ω)

Fig. 3.24: Tuning process of TMN with fixed X_1

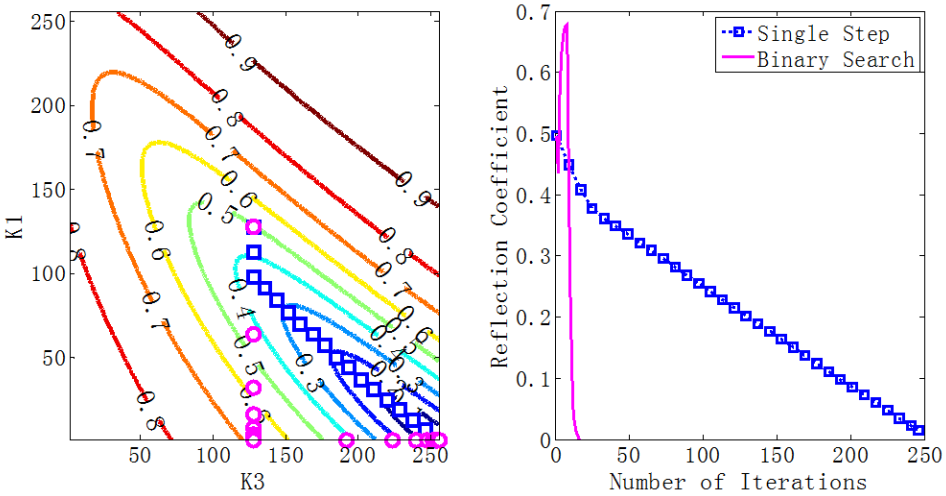
3.7.2 Simulation Results of TMN with Fixed X_2

Tab. 3.3: Tunable matching network with fixed reactance X_2

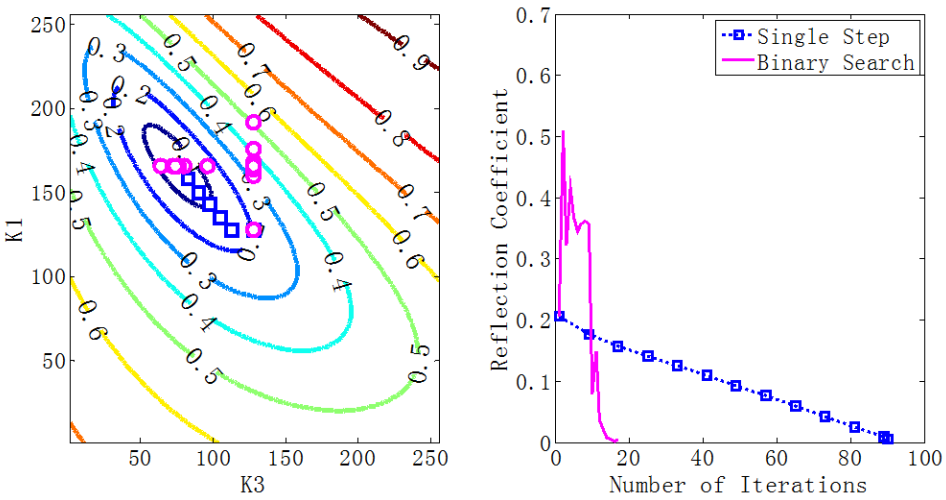
	Resistance (Ω)	Reactance (jΩ)
Source Impedance Z_S	50	0
Load Impedance Z_L	$[30, 100]$	$[0, 100]$
Fixed Inductor X_1	0	$[-126.6, -70.5]$
Tunable Capacitor X_2	0	120.0
Tunable Capacitor X_3	0	$[98.5, 282.3]$



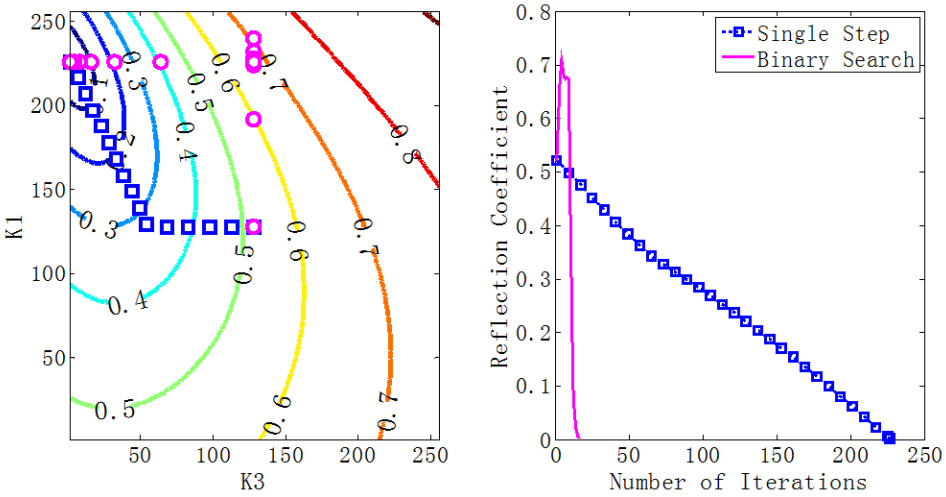
(a) Load Impedance is equal to 30 (Ω)



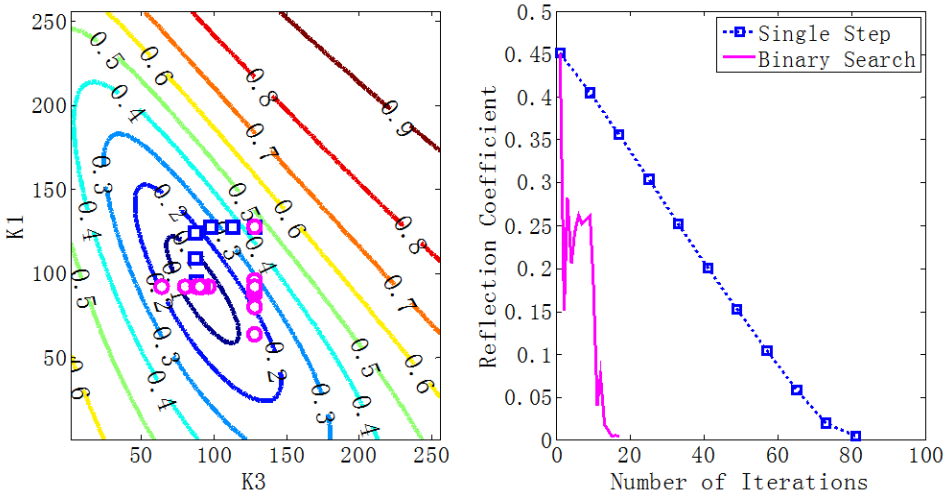
(b) Load Impedance is equal to 30+j100 (Ω)



(c) Load Impedance is equal to 65+j50 (Ω)



(d) Load Impedance is equal to 100 (Ω)



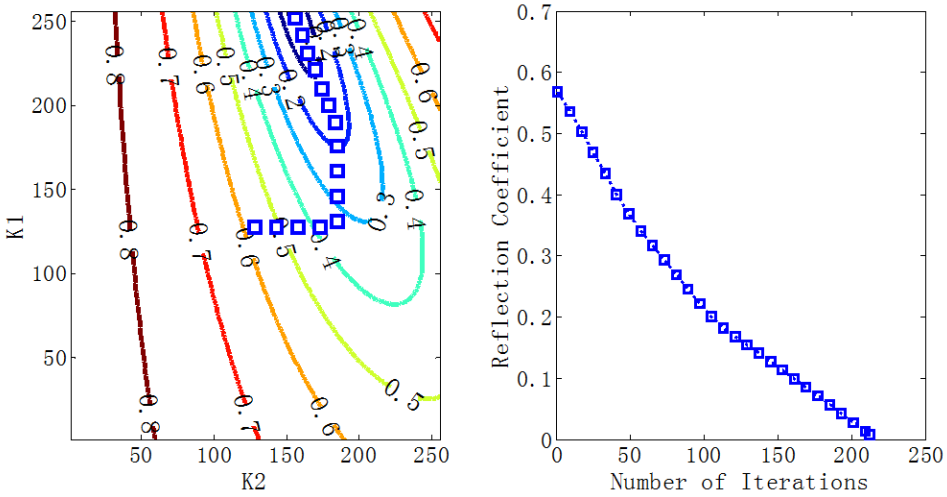
(e) Load Impedance is equal to 100+j100 (Ω)

Fig. 3.25: Tuning process of TMN with fixed X_2

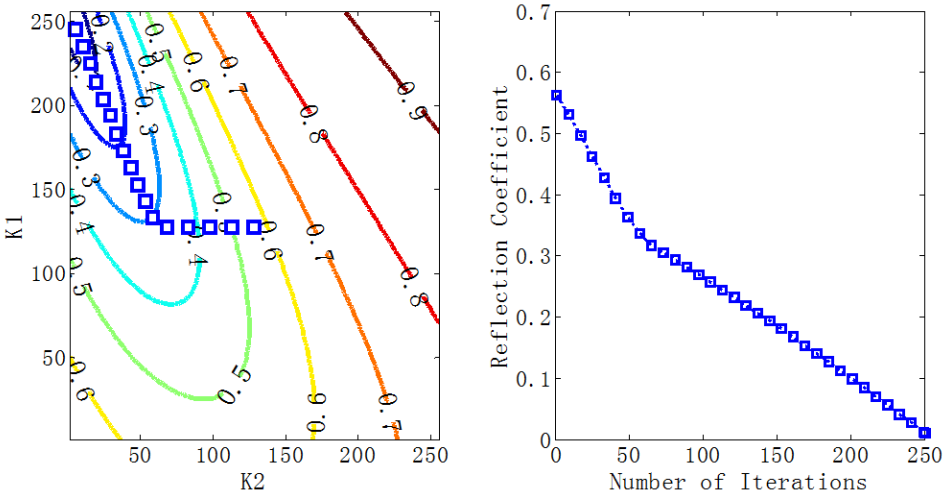
3.7.3 Simulation Results of TMN with Fixed X_3

Tab. 3.4: Tunable matching network with fixed reactance X_3

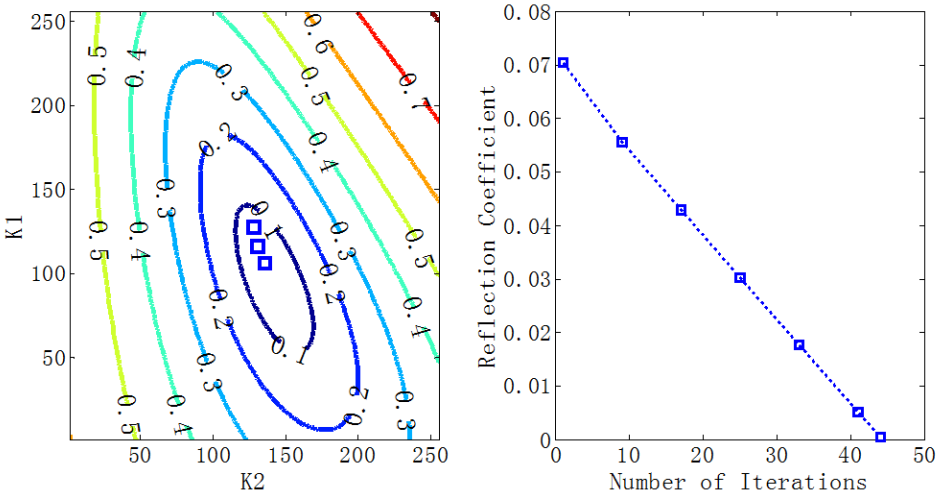
	Resistance (Ω)	Reactance (jΩ)
Source Impedance Z_S	50	0
Load Impedance Z_L	$[30, 100]$	$[0, 100]$
Fixed Inductor X_1	0	$[-90.3, -64.1]$
Tunable Capacitor X_2	0	$[3.6, 169.7]$
Tunable Capacitor X_3	0	130.0



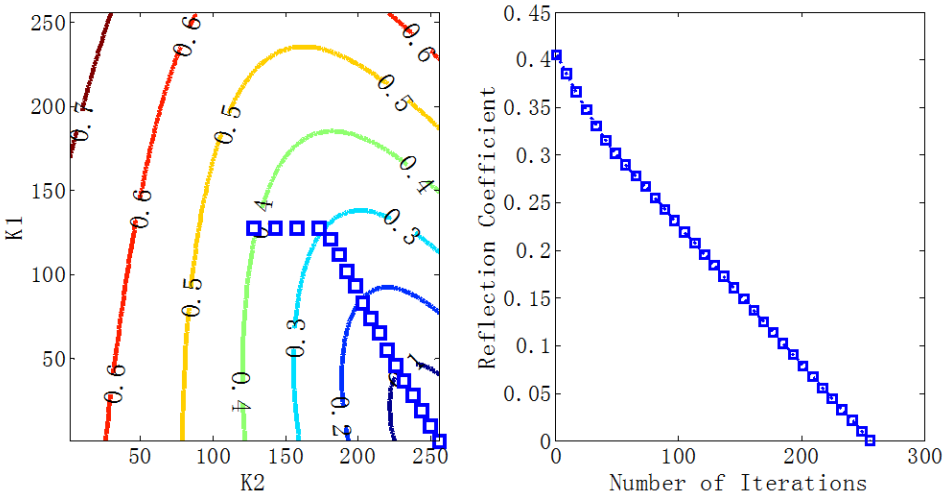
(a) Load Impedance is equal to 30 (Ω)



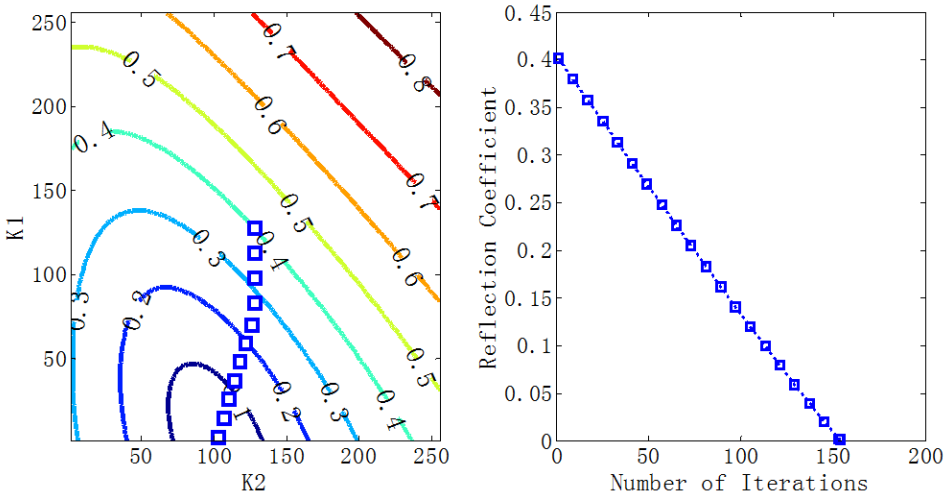
(b) Load Impedance is equal to 30+j100 (Ω)



(c) Load Impedance is equal to 65+j50 (Ω)



(d) Load Impedance is equal to 100 (Ω)



(e) Load Impedance is equal to 100+j100 (Ω)

Fig. 3.26: Tuning process of TMN with fixed X_3

3.8 Further Discussion: Lossy Matching Network

3.8.1 Insertion Loss: S_{21}

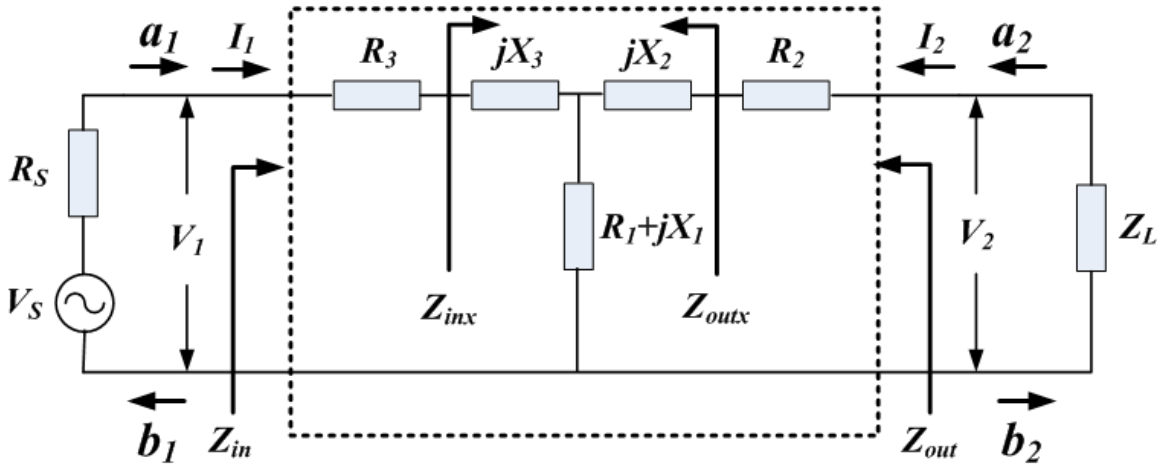


Fig. 3.27: Lossy T-type matching network

In case of lossy network, the source match and load match cannot be achieved simultaneously. Additionally, it is necessary to evaluate the insertion loss caused by the parasitic resistance. As shown in Fig.3.27, the insertion loss is written as

$$S_{21} = \frac{2\sqrt{R_S R_L} \times Z_1}{(Z_L + Z_2 + Z_1) R_S + (Z_L + Z_2 + Z_1) Z_3 + (Z_L + Z_2) Z_1} \tag{3.48}$$

3.8.2 R_1 is equal to zero

If R_1 is equal to zero, we should transform the equivalent load impedance ($R_2 + Z_L$) to the equivalent source impedance ($R_S - R_3$).

$$R_s = Z_{in} = Z_{inx} + R_3 \tag{3.49}$$

$$\hat{Z}_L = Z_L + R_2 \tag{3.50}$$

3.8.3 R_1 is not equal to zero

If R_1 is not equal to zero, the input impedance of lossy Γ-type matching network is rewritten as

$$\hat{Z}_{in} = \frac{(R_1 + jX_1)\left(\hat{R}_L + jX_L + jX_2\right)}{R_1 + \hat{R}_L + j(X_L + X_1 + X_2)} \tag{3.51}$$

The equation (3.51) can be viewed as a linear fractional transformation. Hence, the same analysis can be reused. However, the calculation process could be very tedious and complicated. To simplify the calculation process, the impact of R_1 on the input impedance of Γ-type network is written as

$$\frac{\hat{Z}_{in}(R_1 \neq 0)}{\hat{\mathrm{Z}}_{in}(R_1 = 0)} = \frac{(R_1 + jX_1)\left(\hat{R}_L + jX_L + jX_2\right)}{R_1 + \hat{R}_L + j(X_L + X_1 + X_2)} \times \frac{\hat{R}_L + j(X_L + X_1 + X_2)}{jX_1\left(\hat{R}_L + jX_L + jX_2\right)} \tag{3.52}$$

Since X_1 is much larger than R_1, the equation (3.52) can be simplified as

$$\frac{\hat{Z}_{in}(R_1 \neq 0)}{\hat{\mathrm{Z}}_{in}(R_1 = 0)} \approx \frac{\hat{R}_L + j(X_L + X_1 + X_2)}{R_1 + \hat{R}_L + j(X_L + X_1 + X_2)} \tag{3.53}$$

Therefore, if $R_L + R_2 >> R_1$ or $|X_L + X_1 + X_2| >> R_1$, the impact of R_1 on the input impedance can be ignored. Hence, the proposed convergence criteria can be used in the lossy network. Additionally, as shown in Fig.3.28, the matching region is slightly changed by R_1. The R_1 can result in a mismatch. To secure that the matching region can fully cover the area of complex conjugate of load impedance, we can expand the matching region.

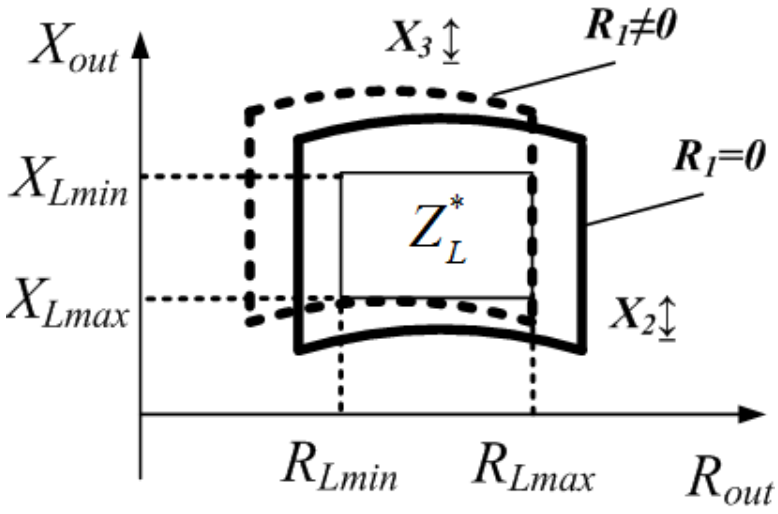


Fig. 3.28: The mismatch caused by the parasitic resistance R_1

3.8.4 Design Strategy of Lossy Matching Network

(1) Assume that the matching network is lossless, calculate the network parameters X_1, X_2, and X_3 with proposed design strategy in section 3.4.

(2) Estimate R_1, R_2, and R_3.

(3) Calculate the equivalent load impedance and source impedance.

(4) Redesign the matching network with equivalent R_S and Z_L, and then calculate the new network parameters X_1, X_2, and X_3.

3.8.5 Simulation Results of Lossy Matching Networks

This section redesigns the tunable matching network in section 3.7 and quantifies the efficiency of lossy matching network.

(1) Assume the matching network is lossless. As shown in Tab.3.5, all load impedance points are calibrated and insertion loss is zero.

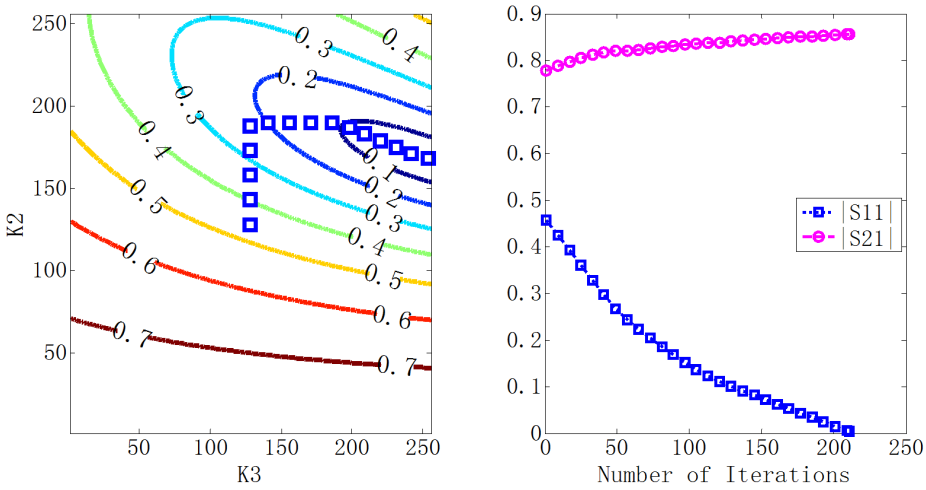
Tab. 3.5: Tunable lossless matching network with fixed reactance X_1

Network Parameters (Ω)	Z_L (Ω)	R_L (dB)	I_L (dB))
$R_L \in [30, 100]$	30	44.1	0.0
$X_L \in [0, 100]$	30+j50	44.4	0.0
$R_S = 50$	30+j100	44.6	0.0
$R_1 = 0$	65	65.4	0.0
$R_2 = 0$	65+j50	62.9	0.0
$R_3 = 0$	65+j100	60.9	0.0
$X_1 = -141.4$	100	117.6	0.0
$X_2 \in [146.8, 314.6]$	100+j50	77.8	0.0
$X_3 \in [228.0, 317.0]$	100+j100	71.9	0.0

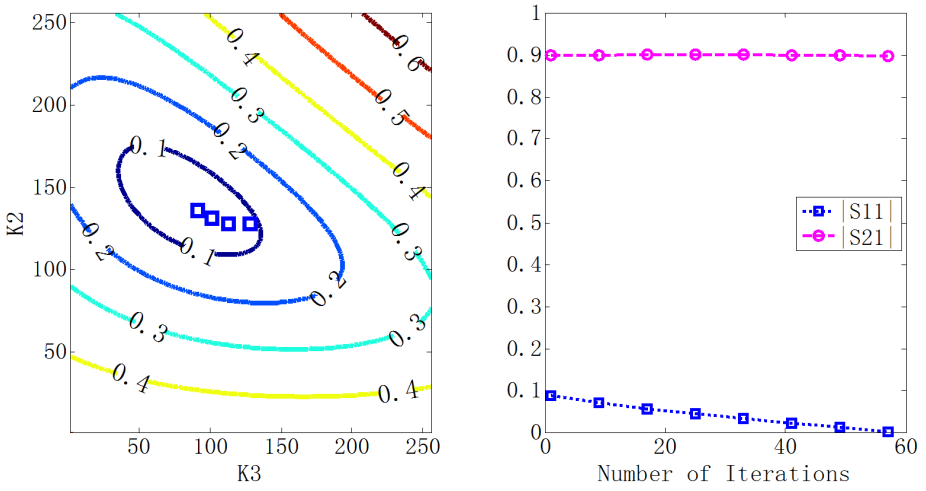
(2) Estimate R_1, R_2, and R_3; redesign the matching network with equivalent load impedance and source impedance. As shown in Tab.3.6, if R_1 is zero, the matching network can reach the perfect matching point.

Tab. 3.6: Tunable lossy matching network-I with fixed reactance X_1

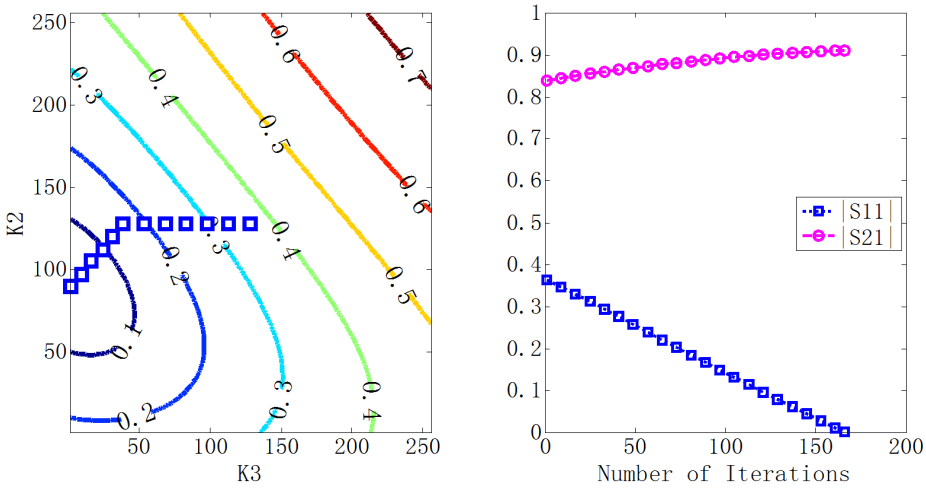
Network Parameters (Ω)	Z_L (Ω)	R_L (dB)	I_L (dB))
$R_L \in [30, 100]$	30	48.7	1.35
$X_L \in [0, 100]$	30+j50	47.8	1.35
$R_S = 50$	30+j100	46.8	1.35
$R_1 = 0$	65	56.6	0.94
$R_2 = 6$	65+j50	58.5	0.94
$R_3 = 6$	65+j100	60.8	0.94
$X_1 = -122.9$	100	118.3	0.81
$X_2 \in [128.1, 281.6]$	100+j50	72.7	0.81
$X_3 \in [188.8, 251.5]$	100+j100	66.7	0.81



(a) $Z_L = 30\Omega; Optimum|S_{21}| = 0.8592; Actual|S_{21}| = 0.8561$



(b) $Z_L = 65 + j50\Omega; Optimum|S_{21}| = 0.9041; Actual|S_{21}| = 0.8974$



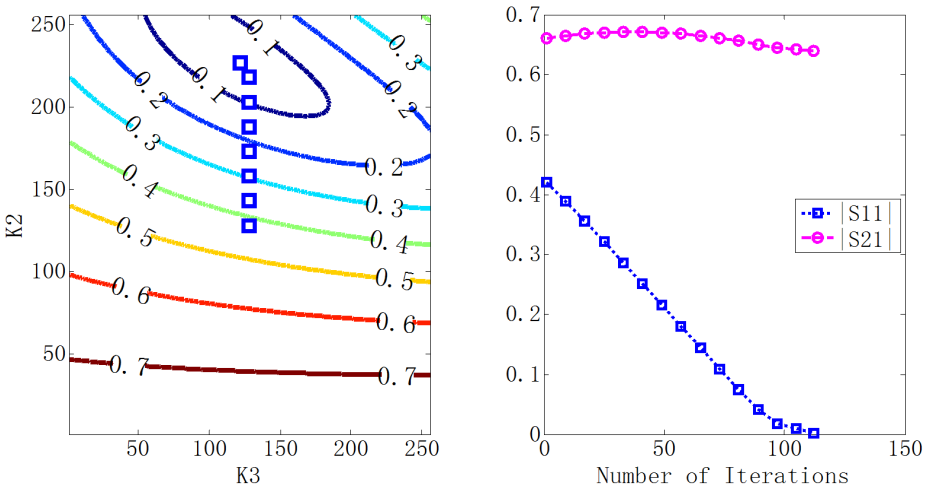
(c) $Z_L = 100 + j100\Omega; Optimum|S_{21}| = 0.9178; Actual|S_{21}| = 0.911$

Fig. 3.29: Tuning process of lossy TMN-I

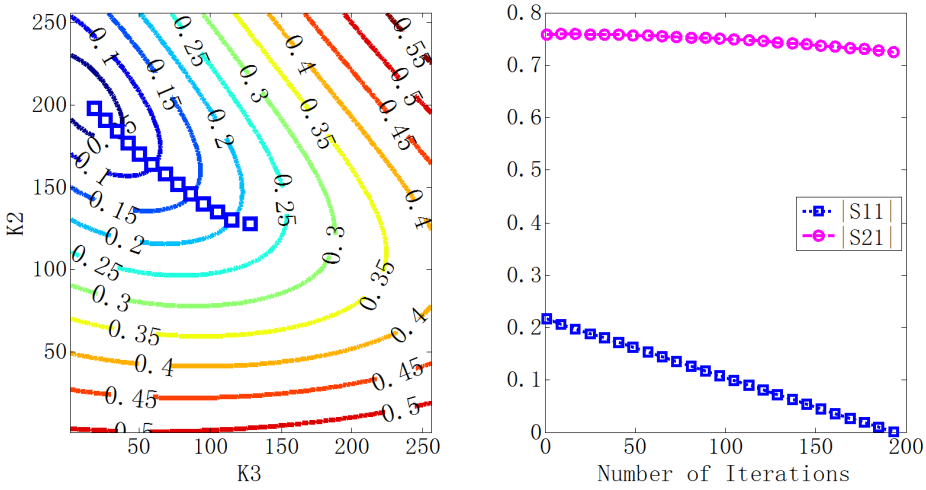
If R_1 is not zero, the matching region is changed slightly by the non-zero R_1. As shown in Tab.3.7, if R_L is closed to 100Ω, the load impedance cannot be calibrated perfectly. In accordance with section 3.8.3, we can expand the range of matching region to solve this problem. For example, set the R_{Lmax} to be 120Ω.

Tab. 3.7: Tunable lossy matching network-II with fixed reactance X_1

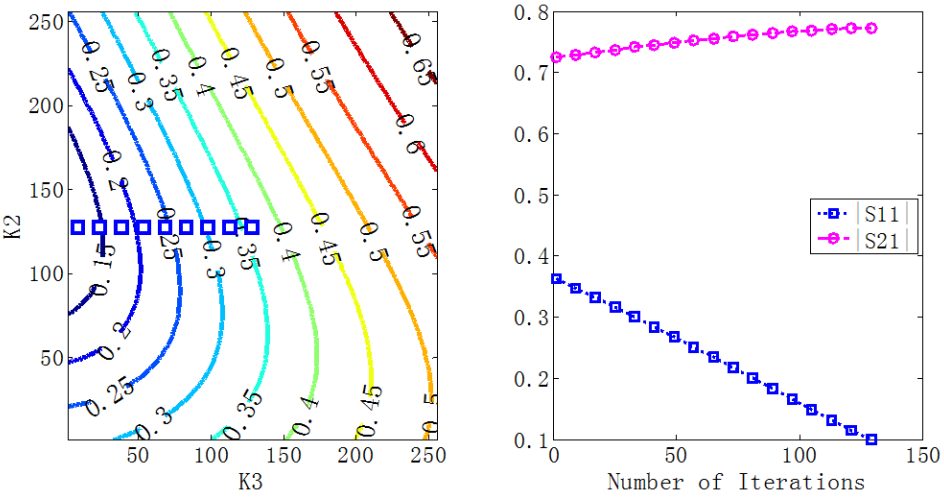
Network Parameters (Ω)	Z_L (Ω)	R_L (dB)	I_L (dB))
$R_L \in [30, 100]$	30	51.7	3.87
$X_L \in [0, 100]$	30+j50	52.2	3.87
$R_S = 50$	30+j100	52.5	3.87
$R_1 = 6$	65	23.9	2.56
$R_2 = 6$	65+j50	60.8	2.79
$R_3 = 6$	65+j100	60.3	2.79
$X_1 = -122.9$	100	17.8	2.03
$X_2 \in [128.1, 281.6]$	100+j50	20.0	2.23
$X_3 \in [188.8, 251.5]$	100+j100	20.0	2.23



(a) $Z_L = 30\Omega; Optimum|S_{21}| = 0.6872; Actual|S_{21}| = 0.6405$



(b) $Z_L = 65 + j50\Omega; Optimum|S_{21}| = 0.7720; Actual|S_{21}| = 0.7253$



(c) $Z_L = 100 + j100\Omega; Optimum|S_{21}| = 0.8081; Actual|S_{21}| = 0.7736$

Fig. 3.30: Tuning process of lossy TMN-II

3.9 Box-Sphere Intersection Testing

This section introduces a simple method for box-sphere intersection testing [17], which is used in the design of tunable matching network with fixed X_2.

Suppose we wish to determine whether a n-dimensional box, B, intersects a n-dimensional sphere with center C and radius r. Denote C by $(C_1,...,C_n)$ and B by closed intervals $[B_{1min}, B_{1max}],...,[B_{nmin}, B_{nmax}]$. We can perform this test by finding a point P on or in the box, which is closest to the center of the sphere. If the distance between the point P and center point C is not greater than radius r, then the box intersects the sphere.

$$Min \quad dis(P) = \sqrt{(C_1 - P_1)^2 + \cdots + (C_n - P_n)^2} \tag{3.54}$$

subject to

$$B_i^{\min} \le P_i \le B_i^{\max} \quad i = 1, ..., n \tag{3.55}$$

The calculation procedure is shown in Fig.3.31.

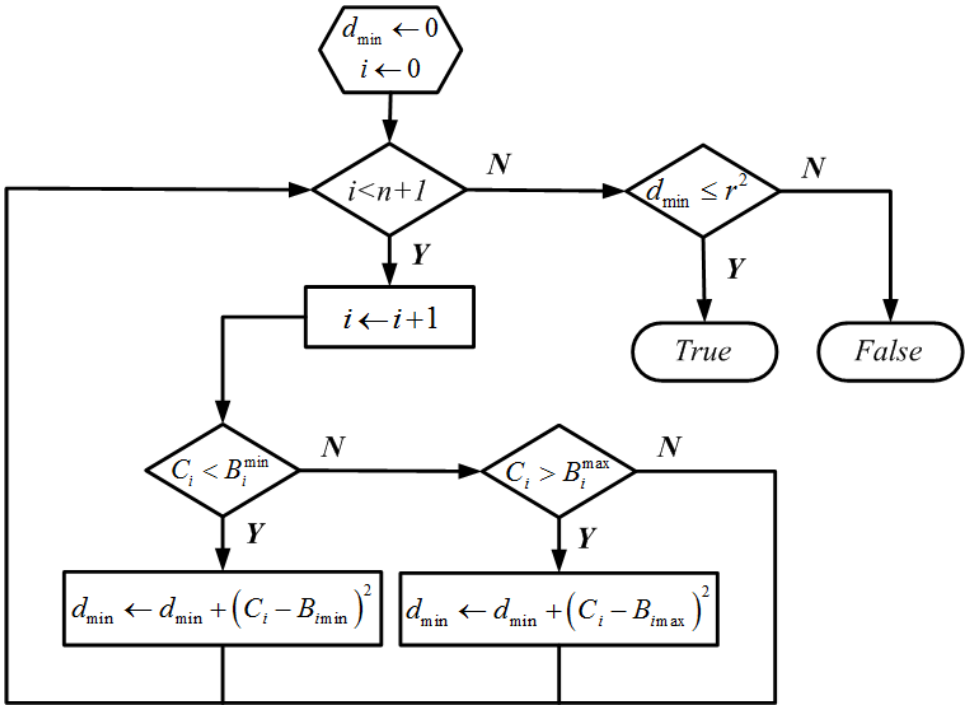


Fig. 3.31: An algorithm for intersecting a solid n-D box with a solid n-D sphere

3.10 Summary

This chapter presents a set of convergence criteria of tunable matching network. Therefore, all matching networks are capable of finding the neighbourhood of matching point. Furthermore, this chapter presents a novel fast tuning algorithm for tunable matching network. In the end, we demonstrate that the proposed methods can be used in the lossy network. A simulation platform of tunable matching network *(SPARTAN)* is designed, which integrates all algorithms in this chapter. The Graphical User Interface (GUI) is shown in Fig.3.32.

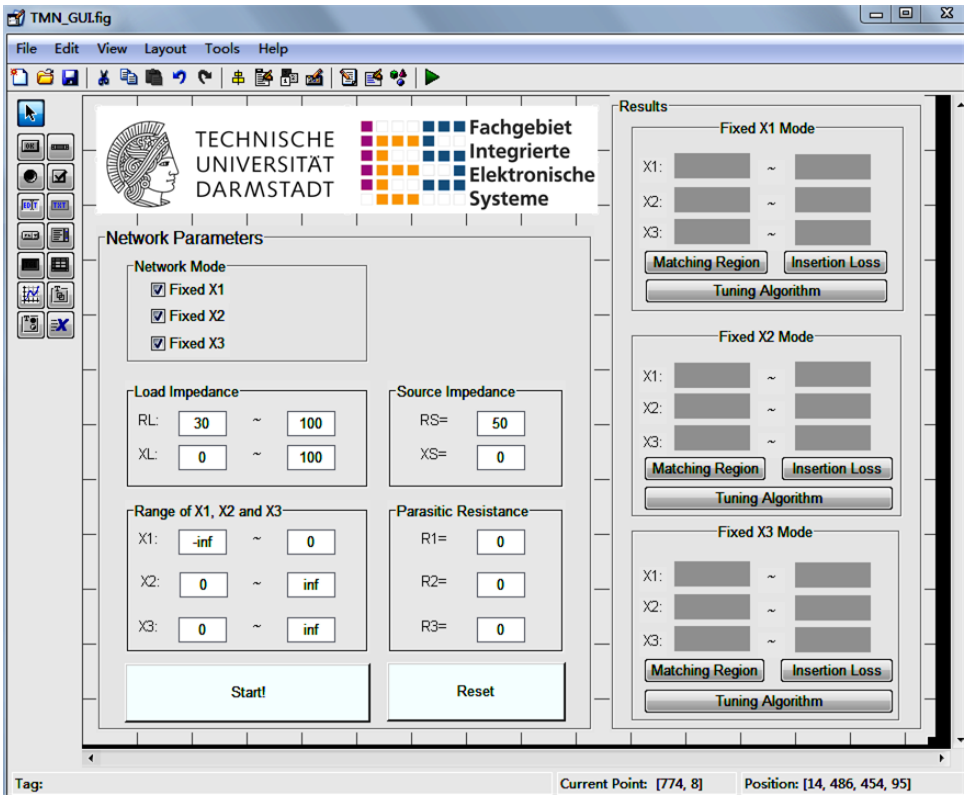


Fig. 3.32: *SPARTAN*

3.11 References

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Chapter 4

Stabilization Charge Pump Method

Contents

4.1 Mathematical Model

A charge pump transforms low input voltage into high output voltage. Common charge pump topologies are the Dickson charge pump [3], the Pelliconi charge pump [4], the heap charge pump, and the Fibonacci charge pump [5,6,7,8]. To achieve the highest voltage gain, the lowest power consumption, and a compact chip size, the Pelliconi charge pump with dynamic bulk-biasing [9] and dead time technology [10] was fabricated. The output voltage of the charge pump is calculated by

$$V_{out} \propto V_{dd} + N \cdot (V_{clk} - \frac{I_L}{2 \cdot \pi \cdot f \cdot C}) \tag{4.1}$$

where I_L stands for the load current, N is the number of charge pump stages, and f is the clock frequency [4,11].

4.2 Power Consumption and Voltage Gain Analysis

The charge pump energy loss falls into four categories: redistribution loss, switching loss, conduction loss, and reversion loss [1,2]. The clock signal affects the switching loss and the reversion loss. The switching loss mainly depends on the clock frequency. The reversion loss is caused by non-ideal clock signals. Dead time technology was involved to reduce the reversion loss. As shown in Fig.4.1, the reverse current flowing from the higher to lower stage is cut off in dead time (*T2, T4*) because all of the switches open shortly between the two charge transfer phases (*T1, T3*). Therefore, voltage gain and power efficiency are improved.

In general, each clock cycle can be divided into two phases: the dead time phase (*T2, T4*) and the charging time phase (*T1, T3*). The capacitors cannot be fully charged because of a short charging time, which in turn decreases the voltage gain. Similarly, the conduction path cannot be cut off completely because of a short dead time, which in turn decreases the voltage gain as well. To obtain the minimum dead time and charging time, the output voltage and power efficiency with different clock schemes are compared in Fig.4.2.

The simulation results demonstrate that the voltage gain and power efficiency have been improved by dead time of 3ns. The 12ns charging time results in a slight voltage drop (marked by an arrow). Therefore, the minimum dead time is 3ns and the minimum charging time is 12ns.

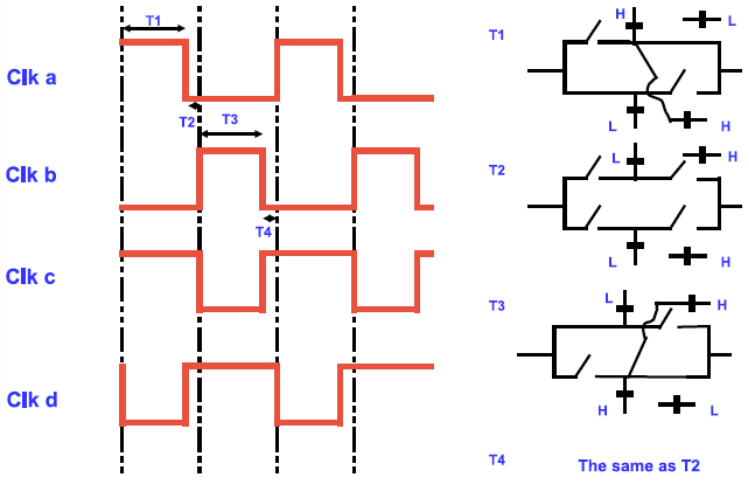

Fig. 4.1: 4-phase clock with dead time technology [11]

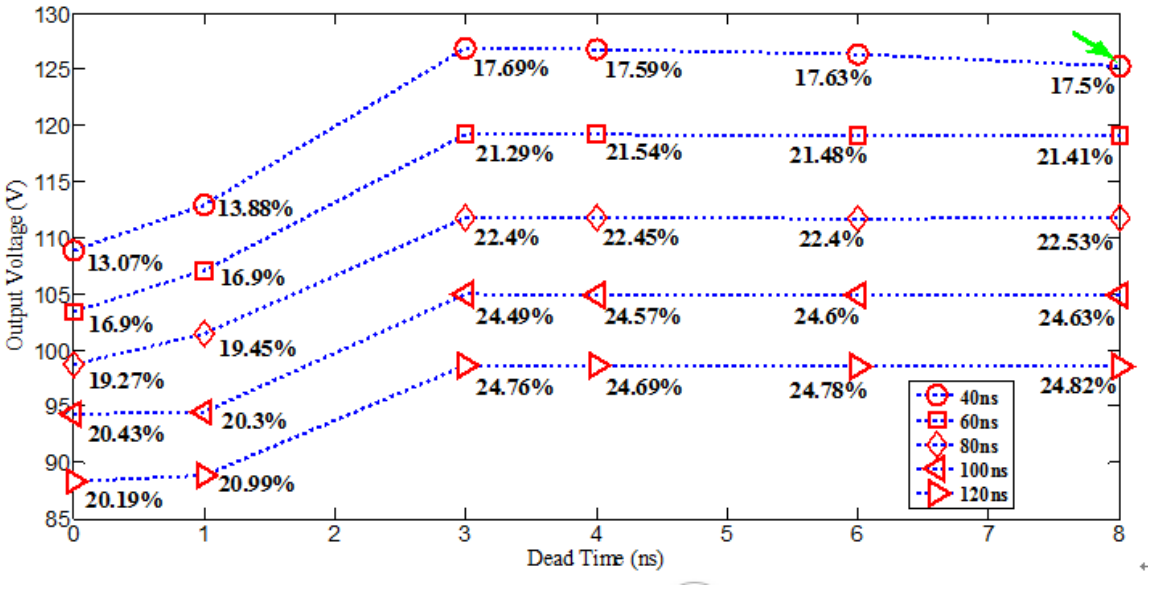

Fig. 4.2: Comparative results - I with different clock parameters

In addition, another 4-phase clock scheme has been proposed [11]. As shown in Figure 4.3, the dead times *T2* and *T4* are divided into two further sub-steps. Similarly, the output voltage and power efficiency with different clock schemes are compared in Fig.4.4 further proving that the minimum dead time is 3 ns and the minimum charging time is 12 ns.

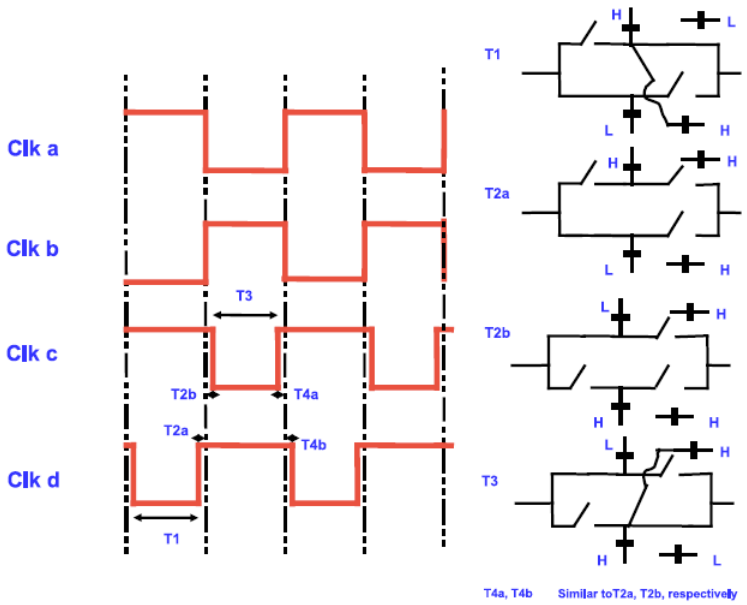

Fig. 4.3: 4-Phase clock with improved controlling of switches [11]

In contrast to Fig.4.1, the second clock scheme does not improve the power efficiency and voltage gain significantly. Moreover, the first clock scheme only requires two groups

of inverted clock signals. Hence, this dissertation focuses on the hardware implementation of a 4-phase clock with dead time technology.

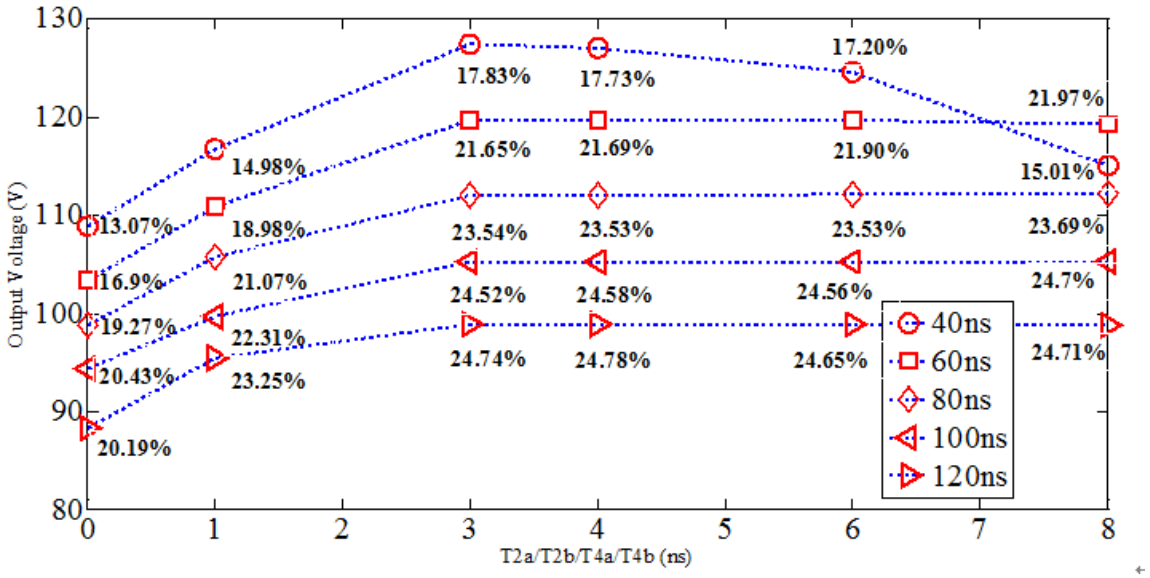

Fig. 4.4: Comparative results - II with different clock parameters

4.3 Counter Based 4-phase Clock Generator

The charge pump output voltage is affected by PVT variations and the dynamic load impedance. The HV-DAC varies its input impedance from 700kΩ to1300kΩ according to the different digital signals. The impact of load impedance and the clock signal on the charge pump output voltage is shown in Tab.4.1.

Tab. 4.1: Output voltage and efficiency of charge pump

V_{dd}, V_{clk}	R_L	*Output Voltage*	*Efficiency*
3.7V	700kΩ	99.54V	25.51%
3.7V	1000kΩ	109.98V	23.65%
3.7V	1300kΩ	116.52V	21.75%
3.6V	1000kΩ	107.01V	23.10%
3.8V	1000kΩ	112.96V	24.41%

To stabilize the charge pump output voltage at 110V, the adaptive 4-phase clock algorithm is shown in Tab.4.2. The dead time is fixed at 4ns. The minimum clock period is 32ns due to the minimum charging time of 12ns and minimum dead time of 4ns. A counter based 4-phase clock generator is designed. As shown in Fig.4.5 and Fig.4.6, the post layout simulations demonstrate the feasibility of the proposed algorithm.

Tab. 4.2: Adaptive 4-phase clock algorithm - I

Initialization: T = 84ns, DeadTime = 4ns, Δ = 4ns;
while(Output Voltage > 111V or Output Voltage < 110 V)
if (Output Voltage > 111V)
T = min(120ns, T+Δ);
else
T = max(32ns, T-Δ);
endwhile

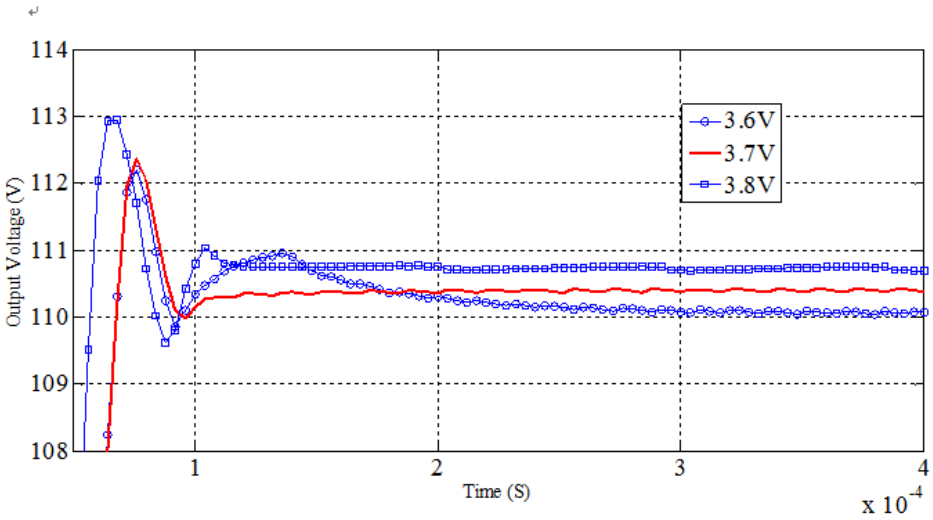

Fig. 4.5: Adaptive 4-Phase clock algorithm - I with different input voltages

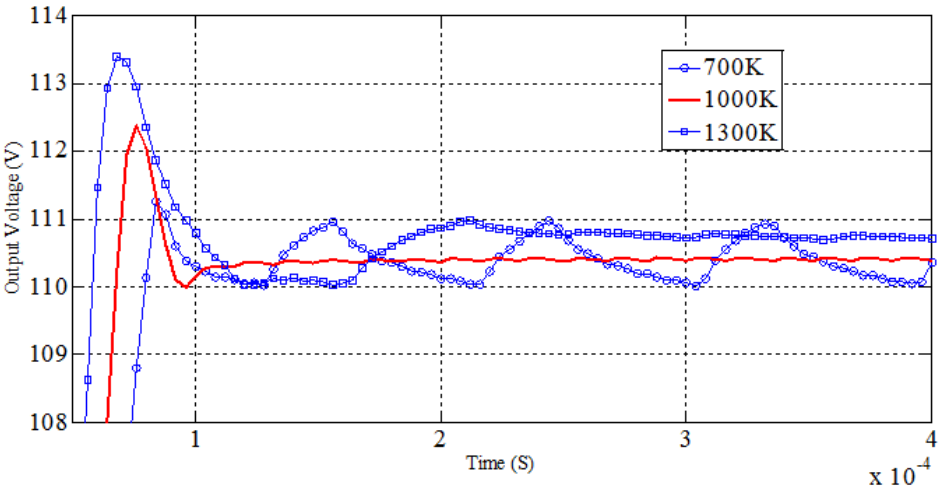

Fig. 4.6: Adaptive 4-Phase clock algorithm - I with different load resistors

4.4 Hybrid DPWM based 4-phase Clock Generator

4.4.1 Motivation

The traditional method is to utilize the clock-counter to generate a 4-phase clock [12]. For AMS H35 technology, the highest clock-counter operating frequency is 250MHz. Therefore, the resolution of the 4-phase clock is 4ns. In the case of a 700 KΩ load resistor, the 4ns resolution results in a voltage variation greater than 1V. As shown in Fig.4.6, the output voltage of charge pump with a 700 KΩ load resistor is fluctuating between 110V and 111V. To achieve more accurate charge pump control, this section proposes a novel hybrid digital pulse width modulator (PWM) that can satisfy the requirements of Tab.4.3.

Tab. 4.3: Adaptive 4-phase clock algorithm - II

Initialization: T = 84ns, DeadTime = 4ns, Δ = 2ns;
while(Output Voltage > 111V or Output Voltage < 110 V)
if (Output Voltage > 111V)
T = min(120ns, T+Δ);
else
T = max(32ns, T-Δ);
endwhile

4.4.2 State-of-the-Art

The traditional method of creating PWM signals is to utilize a fast-clocked counter [12]. The tapped delay line is used to create the PWM signal [13]. The drawback of this method is the use of excessive delay cells. A segmented DPWM architecture is proposed [14]. A hybrid DPWM approach is investigated in [17]. In addition, digital dither approaches have been discussed in [15,16].

The hybrid DPWM with a digital delay locked loop (DLL) requires relatively small hardware resources and can be easily synchronized to an external clock. However, the conventional hybrid DPWM [17] cannot satisfy the requirements of Tab.4.3. Therefore, a novel hybrid DPWM will be discussed in this section.

4.4.3 Delay Cell with Adjustable Time Delay

To control the total delay of the delay line, the delay through each individual delay cell should be adjustable. As shown in Fig.4.7, the proposed delay cell can obtain 1ns time delay with different control signals S[2:0]. There are 8 parallel branches that connect the input port to the 8-bit multiplexer. The first branch consists of 2 delay-units and the last branch consists of 9 delay-units. The control signals S[2:0] are provided by the clock edge detector. In the end, one delay unit is attached at the output of the 8-bit multiplexer improving the clock slew rate. This is due to the fact that the delay-unit consists of two clock inverters. As shown in Fig.4.8, the rise time is reduced by this method.

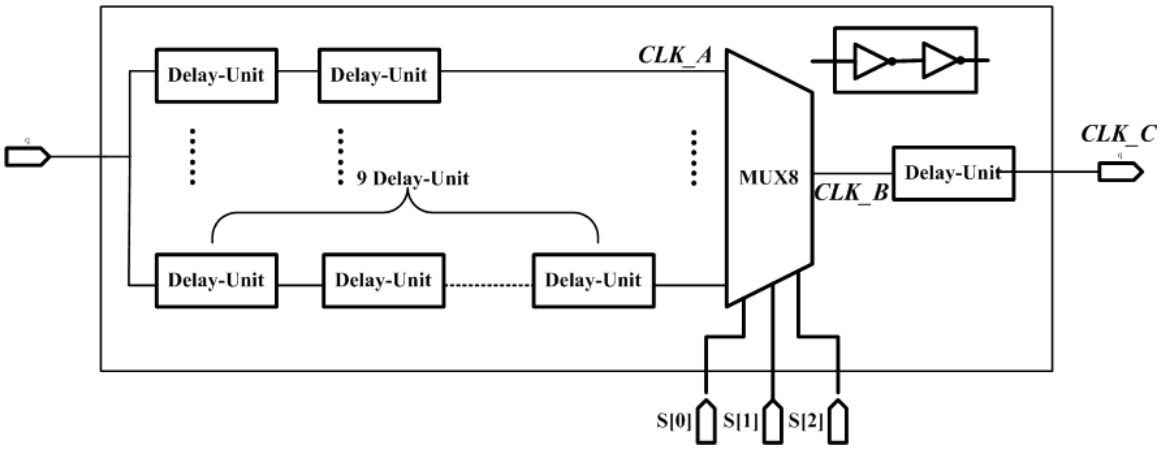

Fig. 4.7: Delay cell module with adjustable time delay

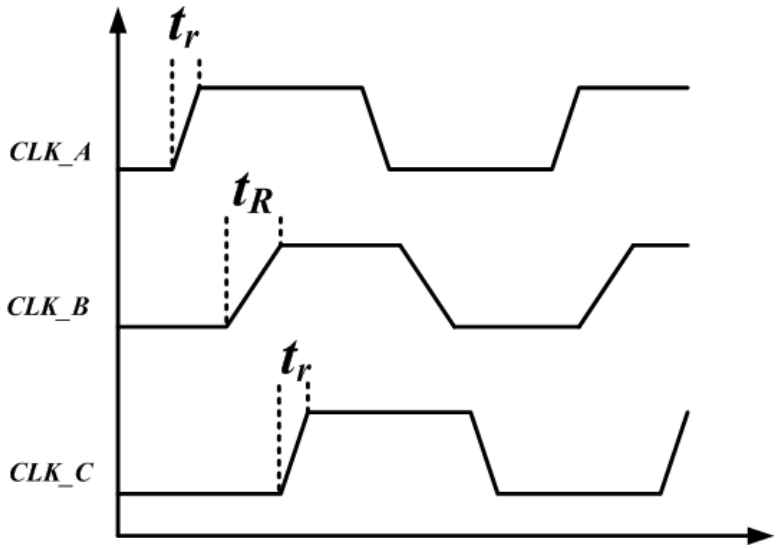

Fig. 4.8: Timing diagram of delay cell

4.4.4 Digital Delay-Locked Loop

The delay line consists of 11 delay cells. The desired delay of each delay cell is 1ns. However, the delay will be affected by PVT variations. To solve this problem, the delay-locked loop (DLL) was used in [17]. As shown in Fig.4.9, the reference clock period is 12ns. Therefore, the delay of CLK6 through the delay line should be equal to 6ns. In other words, the falling edge of CLK0 should be aligned with the rising edge of CLK6. To detect the misalignment between CLK0 and CLK6, a flip-flop was used. As shown in Fig.4.9, if a high value of CLK6 is detected at the falling edge of CLK0, the delay through the first six delay cells should be increased. As a result, the CLK6 will be shifted to the right side. Similarly, if a low value of CLK6 is detected at the falling edge of CLK0, the delay through the first six delay cells should be decreased. As a result, the CLK6 will be shifted to the left side.

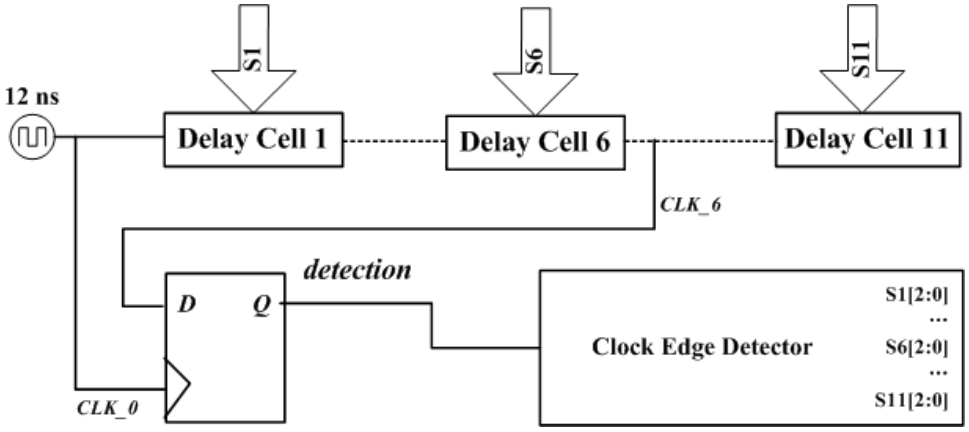

Fig. 4.9: Clock edge detection circuit

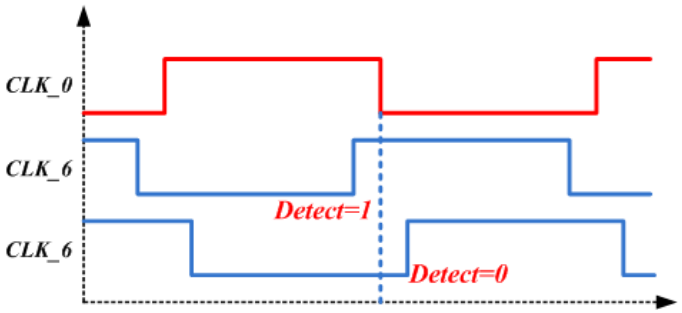

Fig. 4.10: Clock edge detection principle

The clock edge detector is used to adjust the delay through the entire delay line. First, the clock edge detector selects the shortest delay line so that the rising edge of CLK6 is on the left side of the falling edge of CLK0. Second, the clock edge detector increases the delay line to shift CLK6 to the right side. The transition from logic 1 to logic 0 at the flip-flop output indicates that CLK6 has been successfully aligned with CLK0. As a result, the delay of each delay cell is 1ns.

4.4.5 Hybrid Digital Pulse Width Modulator

According to the preceding discussion, the delay between two adjacent clock signals (CLK0,...,CLK11) is 1ns. As shown in Fig.4.11, the control-module outputs one square pulse (CLK0). The square pulse propagates along the delay line and generate a series of clock signals (CLK1,...,CLK11). This process is called coarse tuning. After coarse tuning, the control-module needs to select one clock signal (CLKT) from CLK0 to CLK11. This process is called fine tuning. The Hybrid DPWM timing diagram is shown in Fig.4.12.

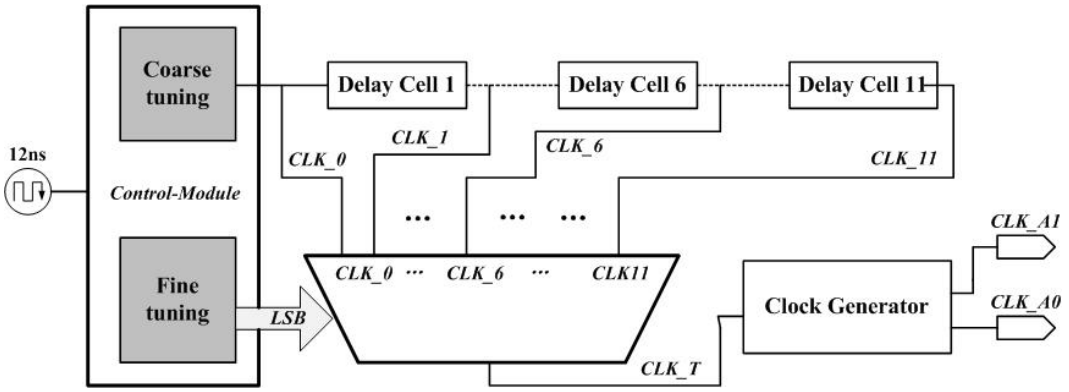

Fig. 4.11: Hybrid DPWM Architecture

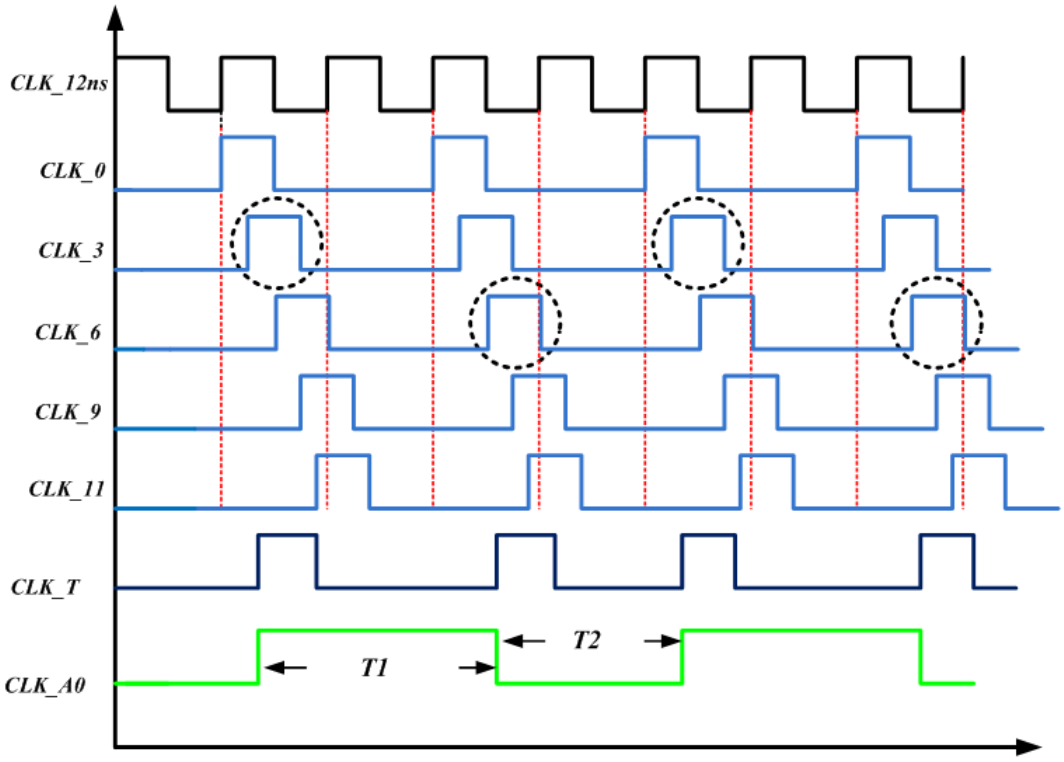

Fig. 4.12: Timing Diagram of Hybrid DPWM

In addition, this method requires that T1 and T2 should be larger than 12ns, the clock period of CLKA0 should be larger than 24ns, and the time resolution is 1ns.

4.4.6 The 4-Phase Clock Generator

As shown in Fig.4.13, the eight delay cells (B1,...,B4,C1,...,C4) have been integrated. The delay of each delay cell is 1ns. Therefore, the delay between CLKA0 and CLKB0 is 4 ns. In the end, CLKB0, CLKB1, CLKD0 and CLKD1 in Fig.4.14 are identical to CLK_a, CLK_d, CLK_b and CLK_c in Fig.4.1.

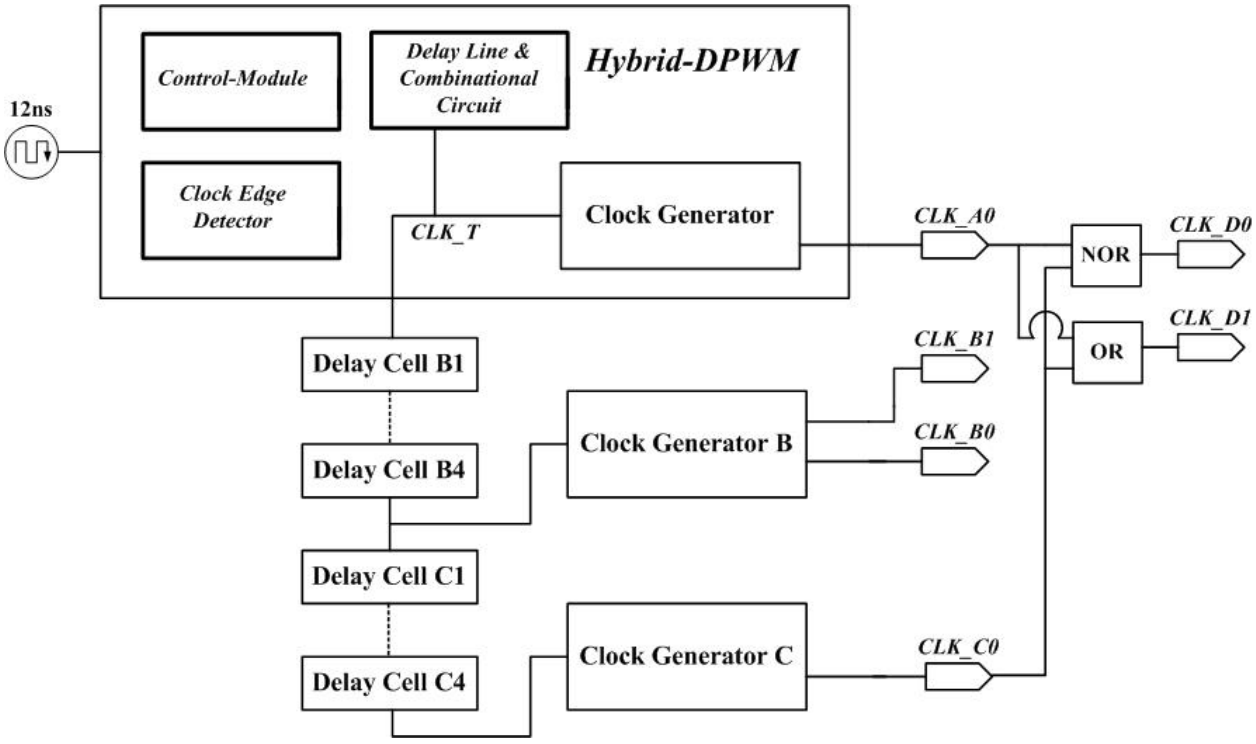

Fig. 4.13: 4-phase Clock Generator

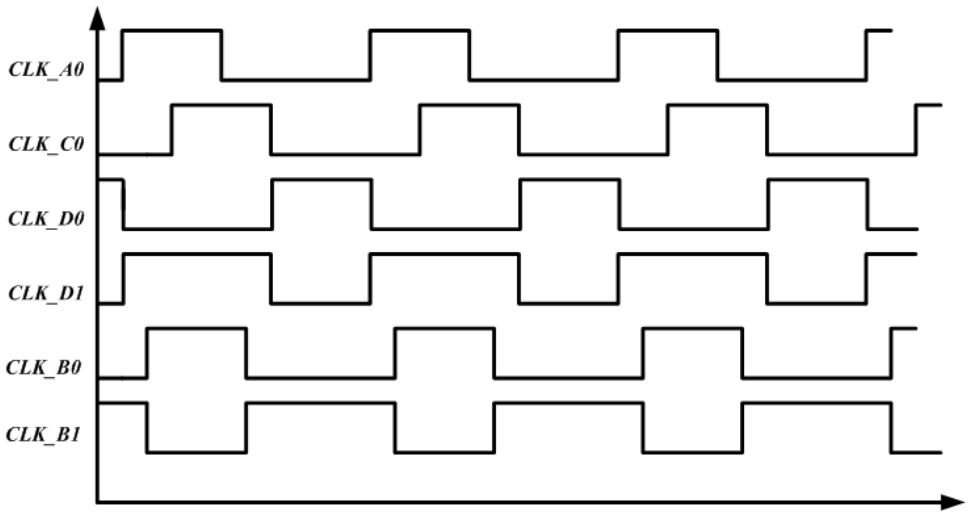

Fig. 4.14: Timing Diagram for 4-phase Clock Generator

4.4.7 Layout and Simulation Results

The proposed method has been implemented in AMS H35 technology. The chip size is $0.53mm^2$, and power consumption is approximately 3mW. According to the post layout simulation, the clock period and dead time are 50ns and 4.2ns, respectively. The proposed hybrid DPWM based 4-phase clock generator satisfies the requirements of Tab.4.3. In addition, the co-simulation demonstrates that this method can stabilize the charge pump output voltage between 110 V and 111 V. Furthermore, as shown in Fig.4.18, compared with the counter based clock generator, the hybrid DPWM based clock generator can provide a more stable output voltage.

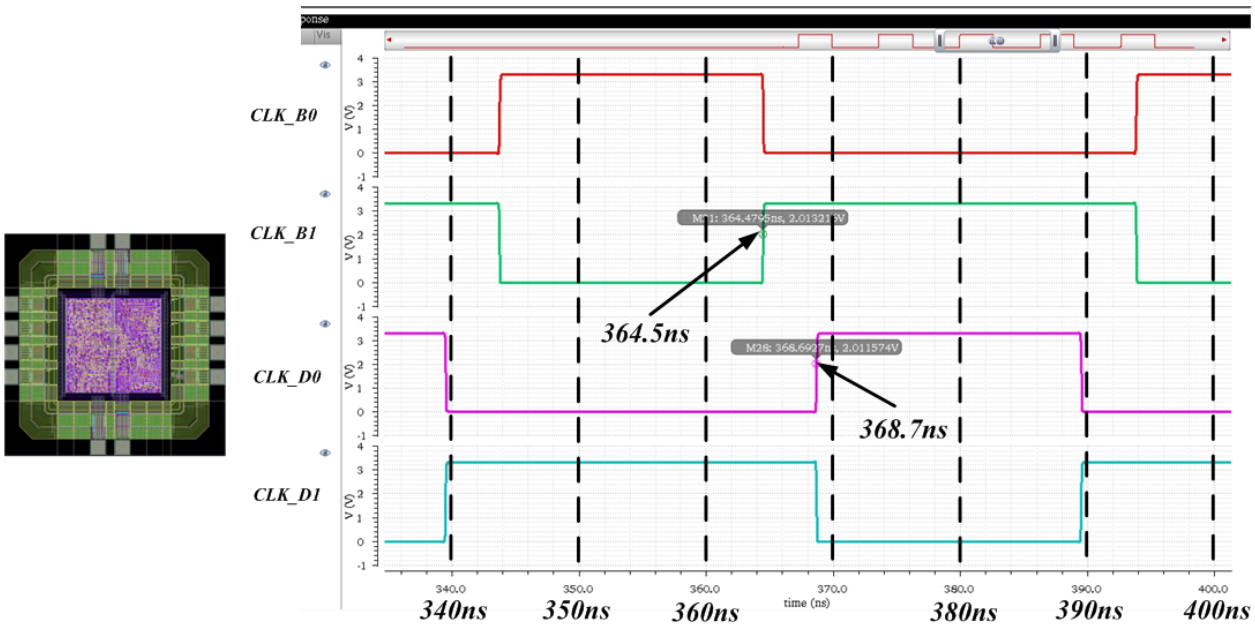

Fig. 4.15: Post layout simulation of proposed hybrid digital pulse width modulator

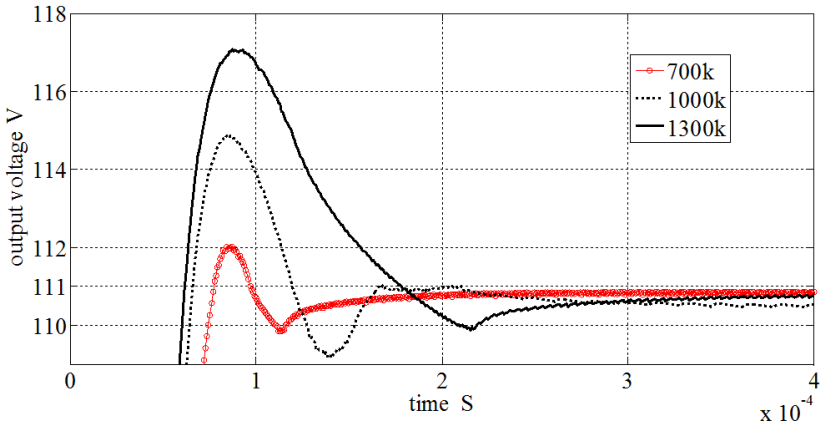

Fig. 4.16: Adaptive 4-Phase clock algorithm - II with different input voltages

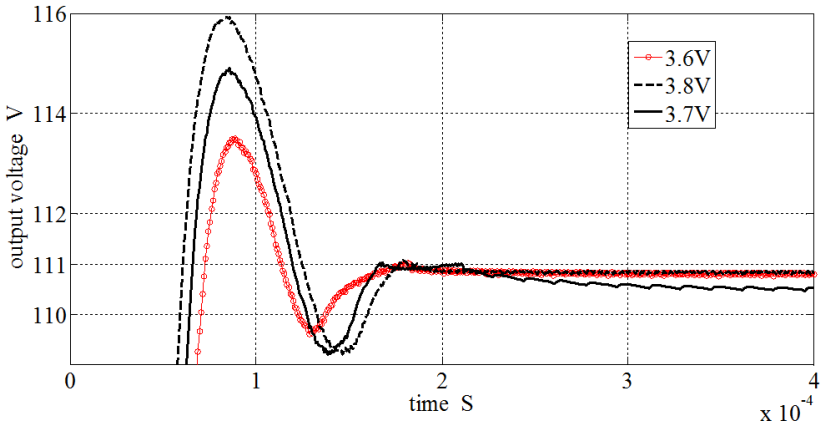

Fig. 4.17: Adaptive 4-Phase clock algorithm - II with different load resistors

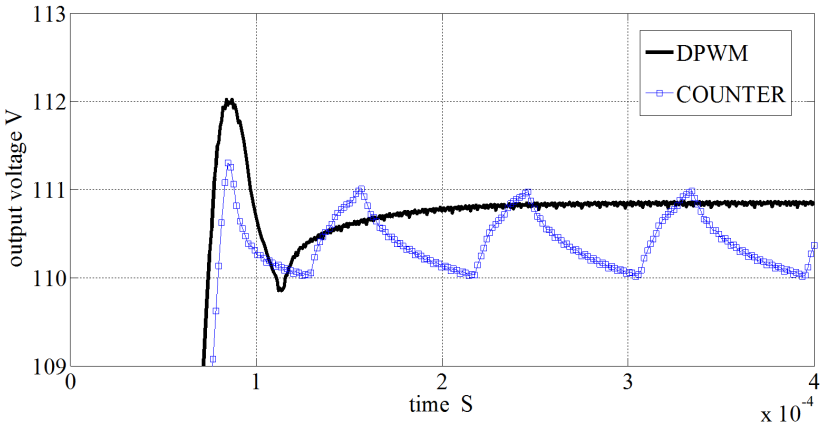

Fig. 4.18: Counter based, Hybrid DPWM based clock generator, 700KΩ load resistor

4.5 References

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Chapter 5

Trade-off Analysis

Contents

5.1 System Review

- *S11 Controller*: As shown in Fig.5.1, the S11 controller consists of one charge pump and two high voltage DACs. The charge pump output voltage is stabilized by the 4-phase clock. The varactors in the tunable matching network are adjusted by the output voltage of the DACs. The chip size and power consumption of charge pump are 17.6mm^2 and 150mW, respectively. The chip size and power consumption of the high voltage DAC are 0.6mm^2 and 18mW, respectively.

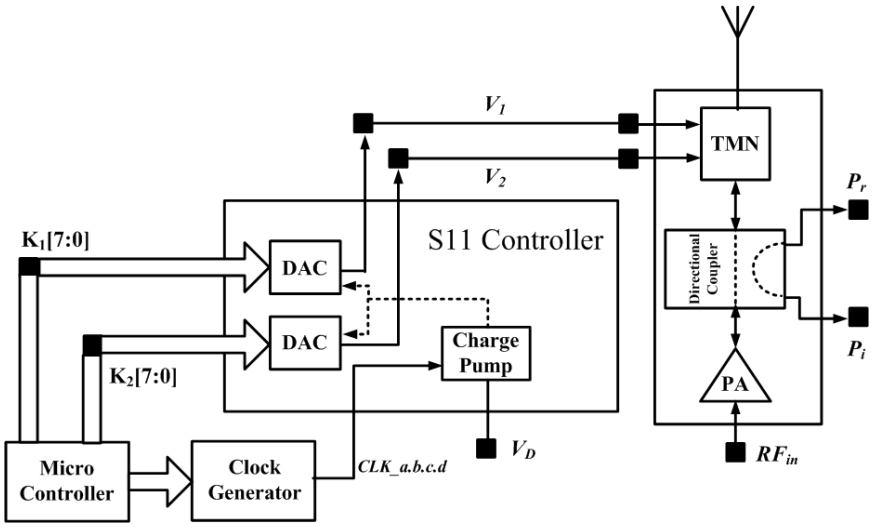

Fig. 5.1: S11 Controller

- *S11 Detector*: The block diagram of the S11 detector is shown in Fig.5.2. The RF detector converts the input power to the output voltage. The S11 parameter is calculated by the analog subtractor. The ADC converts the analog S11 signal to the digital S11 signal. For AMS C35 technology, the area and power consumption of the 12-bit, 1.5MHz ADC are 0.83mm^2 and 8mW, respectively [6]. For 180nm CMOS technology, the area and power consumption of the RF detector working on 5.1GHz are 0.36mm^2 and 10.8mW, respectively [7].

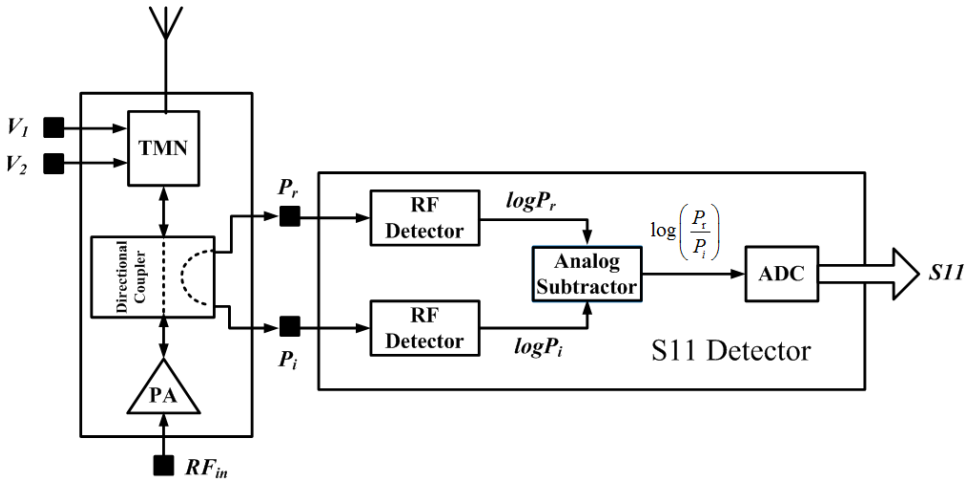

Fig. 5.2: S11 Detector

- *Voltage Detector*: To feedback the charge pump output voltage to the controller, a voltage detector based on XFAB XDH10 was fabricated (data from IES, TU Darmstadt). As shown in Fig.5.3, two resistors R1 and R2 are used to convert V_{CP} ($>$ 100V) to $V_{Divider}$ ($<$ 5V), which is compared with the reference voltage (V_H, V_L). The power consumption of the voltage divider is 16mW due to the high input voltage

($V_{CP} > 100$V). Furthermore, the chip size of the voltage divider is $0.012mm^2$, and the chip size of the voltage comparator is $0.0072mm^2$.

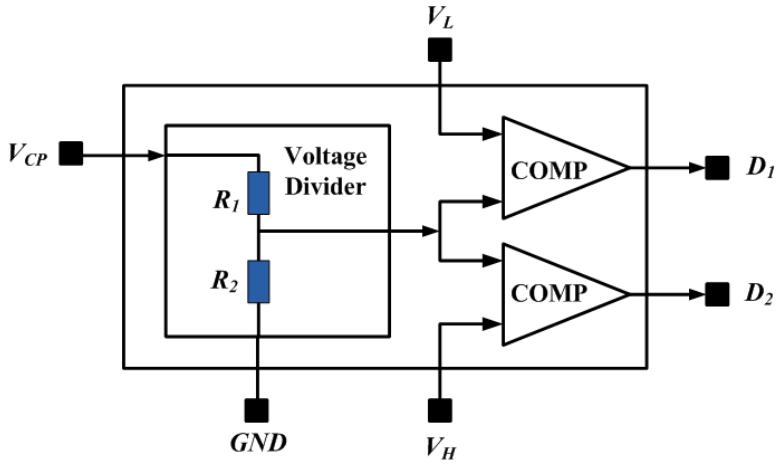

Fig. 5.3: Voltage Detector

- *Cortex-M0 Controller & Clock Generator*: The adaptive impedance matching algorithm and the adaptive 4-phase clock algorithm are performed by a Cortex-M0 controller [1,2,3,4,5], which has been implemented by using AMS H35 technology. According to Appendix B, the controller chip size (including a counter based clock generator) is $2.5mm^2$, the power consumption is 0.32mW/MHz, and the maximum operating frequency is 50MHz. In the case of 50MHz, the running time of the adaptive impedance matching algorithm is less than 3.4ms, and the running time of the adaptive 4-phase clock algorithm is 1.1μs. In addition, the chip size and power consumption of the hybrid DPWM based 4-phase clock generator are $0.53mm^2$ and 3mW, respectively.

5.2 Cost: Area and Power

According to the preceding discussion, the chip areas and power consumption of different components are summarized in the Tab.5.1. The cost of assisted circuits is acceptable due to the expensive charge pump.

Tab. 5.1: Comparison of different building blocks

	Chip Size (mm^2)	Power (mW)	
Charge Pump	17.6	150	
HV 8-bit DAC	0.6	18	
Cortex-M0 (50MHz)	2.5	16	
Clock Generator (DPWM)	0.53	3	
Voltage Detector	0.026	16	
S11 Detector (Estimation)	1.55	29.6	

5.3 Robustness and Design Effort

5.3.1 PVT Variation

Process, voltage, and temperature (PVT) variations have many negative impacts on chip performance [8]. This effect has been increased since the fabrication technology has gone into the deep nanometer scale. (1) Process variations may exist due to variations in channel length or doping concentration. (2) Voltage variations are caused by unexpected voltage drops in the power supply network or variations in the supply voltage itself. (3) Temperature variations arise due to temperature fluctuations and environmental impacts.

However, these negative impacts can be partly solved by digitally assisted analog technology. For example, the clock signal voltage has a significant impact on the charge pump output voltage. A typical analog circuit solution is to design a bandgap voltage reference circuit representing a huge design effort and cost. By using digitally assisted analog technology, the charge pump output voltage can be calibrated by a micro controller. Obviously, the design effort and cost of a voltage detector are much less than the bandgap voltage reference.

In addition, the PVT-induced delay variations affect the timing of the synchronous circuits and lead to time violations. These variations affect both clock signals and data paths. Therefore, the critical stages may fail to deliver their output data within the given clock period. However, the delay variation of delay cells can be calibrated by a controller. For example, the digital delay locked loop is used to calibrate the delay of the delay line. As a result, the delay of each delay cell is 1ns regardless of PVT variations. Compared with analog methods, such as body biasing, the digitally assisted analog method is more attractive.

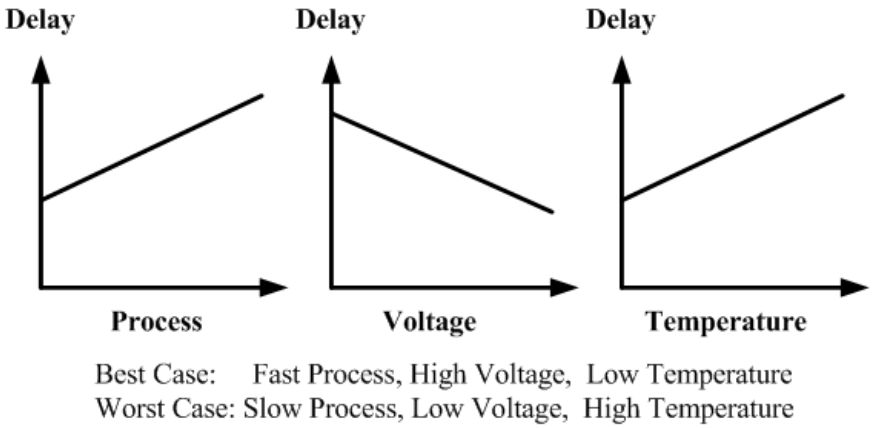

Fig. 5.4: PVT Variations

5.3.2 Nonlinearity

As discussed in chapter 1, the pre-distortion technology can be used to improve the linearity of the power amplifier. In this work, the tunable matching network suffers from the problem of the non-ideal varactors. As shown in Fig.5.6, the relationship between capacitance and voltage is not linear. To solve this problem, the pre-distortion technology can be reused. The block diagram of pre-distortion technology is shown in Fig.5.5.

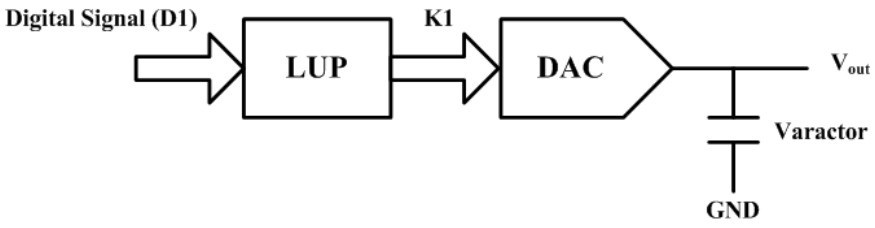

Fig. 5.5: Block diagram of pre-distortion technology

The challenge of this method is the design of the look-up table. The capacitance function of voltage is written as (5.1). The voltage function of signal (K1) is written as (5.2). As a result, the capacitance function of signal (D1) is written as (5.3).

$$C = f_1(V) \tag{5.1}$$

$$V = f_2(K1) = f_2 f_3(D1) \tag{5.2}$$

$$C = f_1 f_2 f_3(D1) \tag{5.3}$$

Because the functions f_1 and f_2 have been determined, the look-up table f_3 is used to make the following equation into a linear function. The calculation procedure is shown in

Fig.5.6. Compared with the design effort of a high linear varactor, updating the look-up table is quite simple.

$$LinearFunction = f_1 f_2 f_3 \tag{5.4}$$

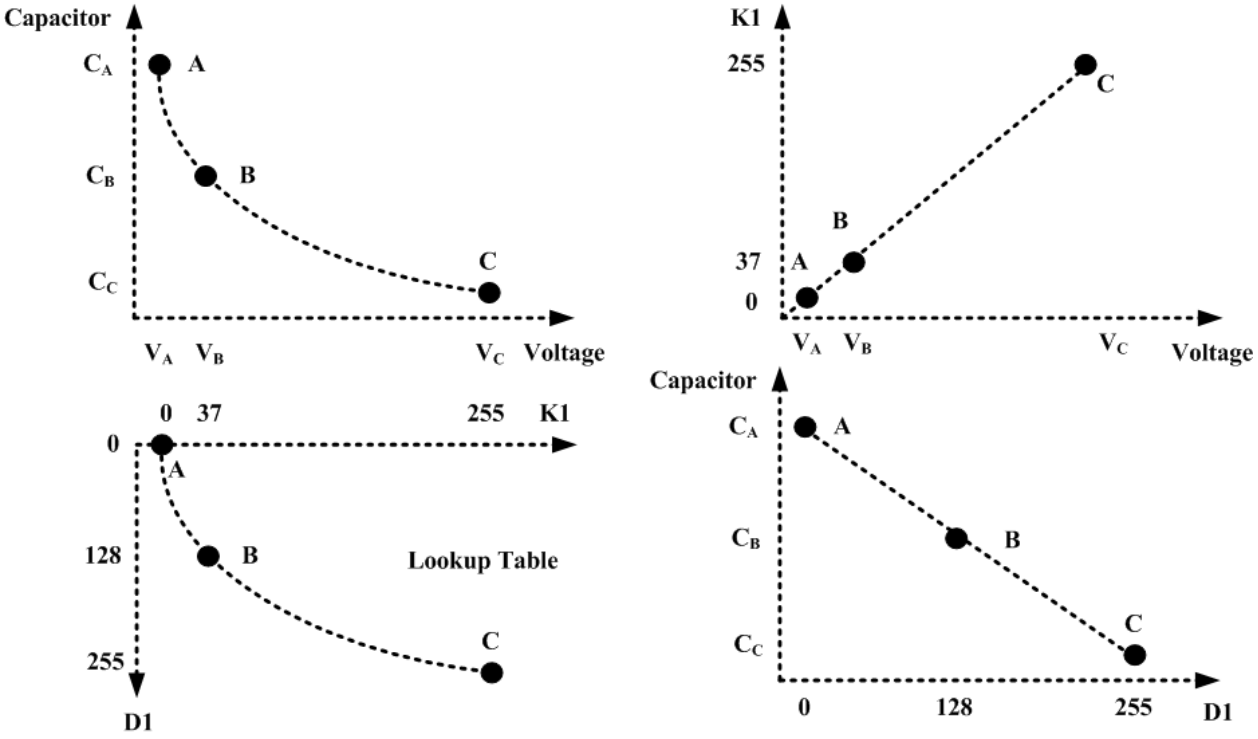

Fig. 5.6: Design strategy of the Look-up table

5.3.3 Mismatch

Impedance matching is very important for RF integrated circuit design. The first reason for matching is power efficiency. The second reason is device protection. If the RF circuit is not matched, we get reflected power. This reflected power builds standing waves on the transmission line, which can destroy the communication system. The digital calibration method can be reused here. As shown in Fig.5.7, by calibrating the tunable matching network with the aid of a controller, the antenna impedance can be matched.

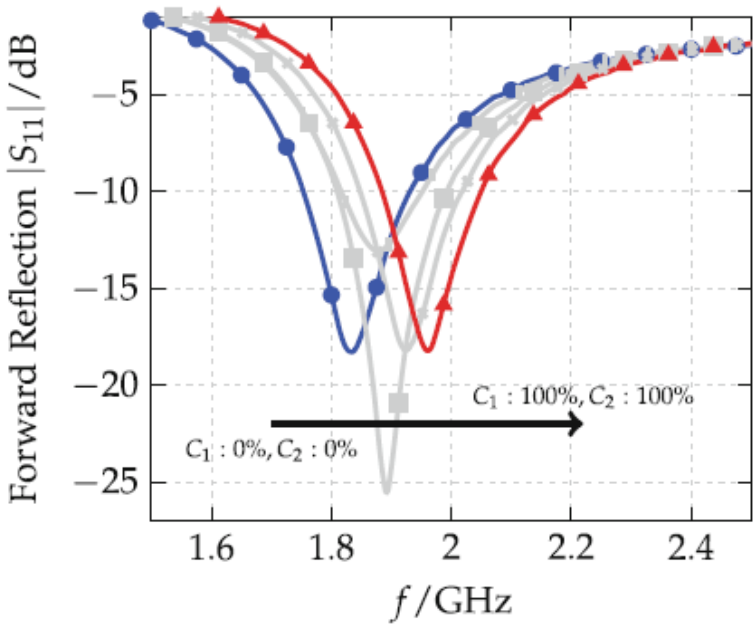

Fig. 5.7: Impedance mismatch [9]

5.4 Trade-offs on Calibration and Compensation

As shown in Fig.5.8, the classification of digitally assisted analog circuits is based on how analog nonidealities are corrected. (1) Digital calibration: adjust analog circuit parameters to calibrate output values of the analog core. (2) Digital compensation: apply the predistortion technology to improve the system accuracy.

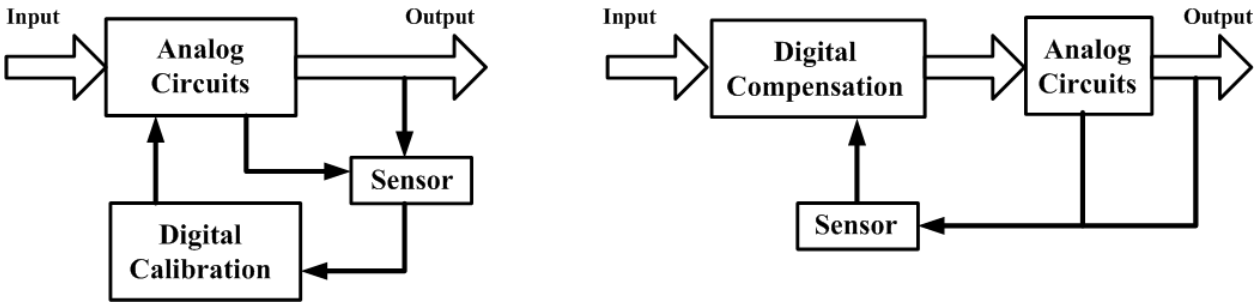

Fig. 5.8: Digital calibration and digital compensation

5.5 References

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Chapter 6

Summary and Outlook

Contents

6.1 Summary

Compared with analog designs, digital designs are faster, smaller and more power efficient as CMOS technologies scale to smaller nodes. Therefore, analog designers take advantage of digital assistant analog technology, which simplifies analog circuits that don't scale easily. Digital calibration or compensation allows for a considerable relaxation of the analog performance, which can be used for minimizing both area and power consumption.

Digitally assisted analog techniques are increasingly needed in future circuit and system designs, as FinFET and FDSOI replace planar CMOS technology at advanced process nodes of 20 nm and beyond. The intrinsic features of these new devices are lowering the barrier between the analog and the digital worlds, allowing unprecedented performance to be achieved by assisting analog circuits with digital techniques [1,2]. The contributions of this dissertation are summarized as follows:

- **Digitally Assisted Charge Pump:** The charge pump cannot stabilize its output voltage at the desired level (110V) due to the PVT variations and dynamic load resistor. Chapter 4 utilizes the adaptive 4-phase clock algorithm to calibrate the charge pump output voltage. Compared with the counter based clock generator (section 4.3), the hybrid DPWM based clock generator (section 4.4) can make the charge pump output voltage more stable (Fig.4.18). Both of these methods require an accurate low

voltage source (e.g. bandgap voltage reference), which will increase the cost and power consumption of this system.

- **Digitally Assisted Tunable Matching Network:** Section 3.7 illustrates that the tunable matching network can be used to calibrate the antenna impedance variation with the aid of the adaptive impedance matching algorithm. The adaptive 4-phase clock algorithm and adaptive impedance matching algorithm are performed by the Cortex-M0 controller (Appendix B). In the case of a 50 MHz operating frequency, the running time of the adaptive impedance matching algorithm is less than 3.4ms. Therefore, the proposed method can be used in the real time system. In addition to this, the Cortex-M0 controller can be shared with other functionalities. Therefore, this method does not require additional cost.

- **Digitally Assisted Varactor:** The varactors can be easily tuned by different voltage. However, the varactors suffer from the non-linearity problem. Section 5.3.2 utilizes the digital pre-distortion method to improve varactor linearity. The pre-distortion algorithm can be easily implemented by using a look-up table.

- **Digitally Assisted Adjustable Delay Cell:** The delay through the adjustable delay cell is affected by the PVT variations. By using a digital delay-locked loop, Section 4.4.4 ensures that the delay through each delay cell is 1 ns.

- **Convergence Criteria of the Tunable Matching Network:** All optimization algorithms are easily trapped into a local optimum point. To solve this problem, Sections 3.4 and 3.5 present a set of convergence criteria for a tunable matching network. As a result, we can converge to the neighbourhood of matching point with high probability, which fulfills the requirements of practical engineering.

- **Fast Tuning Algorithm of the Tunable Matching Network:** As shown in Fig.3.8 and Fig.3.13, the proposed convergence criteria guarantee that the input resistance is proportional to the first tunable component and that input reactance is proportional to the second tunable component. Therefore, Section 3.7 utilizes the binary search algorithm to accelerate the convergence speed. In contrast to the single-step method, the convergence speed is improved from *O(N)* to *O(logN)*.

In this dissertation, digital calibration is applied to correct dynamic non-ideal effects, such as charge pump voltage gain, delay of the delay cell, and the dynamic load impedance of a tunable matching network. Digital compensation is applied to correct static non-ideal effects, such as the nonlinearity of varactors.

The choice between compensation and calibration is not a simple one. From the point of view of area and power consumption, digital calibration is a preferred solution if analog tuning can be implemented with negligible overhead. Compared with digital compensation, digital calibration avoids the constant digital activity. For example, if the charge pump output voltage satisfies the requirement *(110V < Vout < 111V)*, the digital

circuit does not need to perform the 4-phase clock algorithm. If the S11 parameter is less than -10 dB, the digital circuit does not need to perform the adaptive impedance matching algorithm. As a result, this method can reduce energy dissipation. However, some negative effects are difficult to calibrate. For example, compared with the design effort of high linear varactors, digital compensation is a preferred solution from the perspective of design-time.

6.2 Outlook

With the exponential pace of digital performance growth, analog designers are just beginning to understand the potential of digital-processing capabilities. In addition to above examples, digital assistance has found a number of additional applications. Therefore, the researchers are undertaking a paradigm shift from high-precision analog circuits to mixed analog-digital solutions that take advantage of modern IC technology. In this effort, the key to innovation is a broad, multidisciplinary approach using digital-processing capabilities as a driver rather than an afterthought to cope with imperfections in evolutionary analog design [4]. In accordance with the current status of the research results presented in this dissertation, some future work that can be focused on is summarized as follows:

- **Digitally Assisted ADCs:** Digital assisted technology has been widely used in the design of ADCs. Many digital calibration and compensation algorithms are performed by dedicated digital circuits. As shown in Fig.5.2, the ADC is connected to the controller. Hence, some digital calibration and compensation algorithms can be performed by the controller. This method can reduce the chip size and increase the flexibility of the system.
- **Digitally Assisted RF Detectors:** To obtain a large linear-in-dB dynamic range, a digital assistance technique is used to correct the nonlinear output characteristics of RF detectors [3]. This approach includes the compensation of variability effects through self-calibration. Similarly, some digital calibration and compensation algorithms can be performed by the controller.

6.3 References

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Appendix A

Linear Fractional Transformation

According to the conformal mapping method, the central point of linear fractional transformation defined by (3.1) can be calculated by

$$Z_0 = \frac{j}{2} \frac{\begin{vmatrix} b & a \\ d* & c* \end{vmatrix}}{\begin{vmatrix} \mathrm{Re}(d) & \mathrm{Im}(d) \\ \mathrm{Re}(c) & \mathrm{Im}(c) \end{vmatrix}} \tag{A-1}$$

If X_2 is a variable, the equivalent *a*, *b*, *c*, and *d* of (3.2) are written as

$$\begin{cases} a = -X_1 \\ b = -X_L X_1 + jR_L X_1 \\ c = j \\ d = R_L + j(X_L + X_1) \end{cases} \tag{A-2}$$

Furthermore, we can get the equation (3.6). If X_1 is a variable, the equivalent a, b, c, and d of (3.1) are written as

$$\begin{cases} a = -X_L - X_2 + jR_L \\ b = 0 \\ c = j \\ d = R_L + j(X_L + X_2) \end{cases} \tag{A-3}$$

Similarly, the equation (3.11) can be derived.

Appendix B

Design of Cortex-M0 Controller

B.1 The Architecture of Cortex-M0 Processor

B.1.1 System Overview

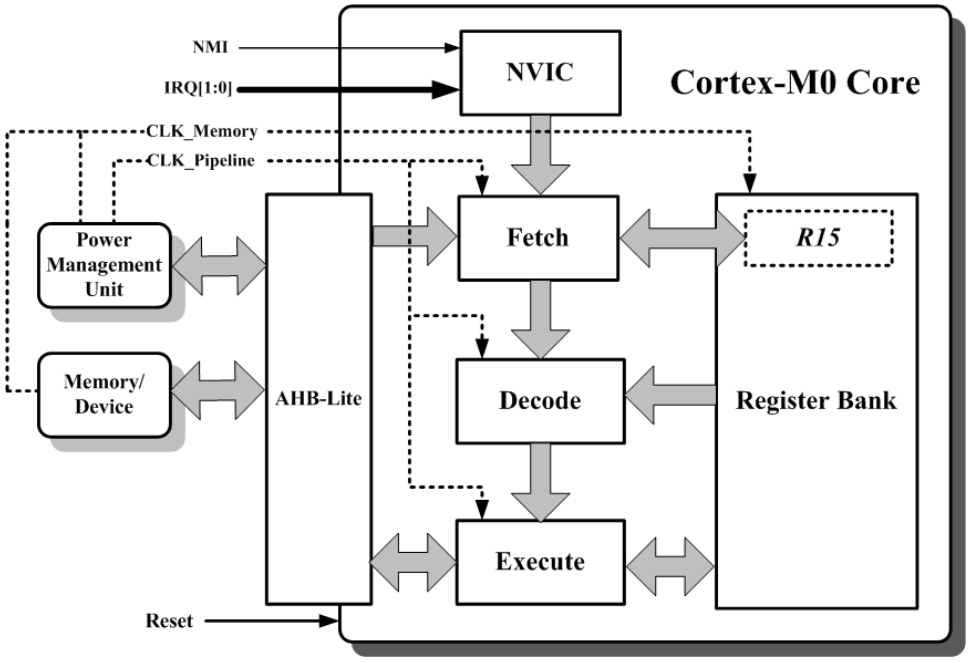

Fig. B.1: The architecture of Cortex-M0 controller

The organization of Cortex-M0 processor is illustrated in Fig.B.1. (1) The instruction is fetched from memory and placed in the instruction pipeline. (2) The instruction is decoded and the datapath control signals are prepared for the next cycle. In this stage, the instruction owns the decode logic but not the datapath. (3) The instruction owns the datapath; the register bank is read/written, an operand is shifted, the ALU result is generated and written back into a destination register. At any one time, three different instructions

may occupy each of these stages. Hence, the hardware in each stage has to be capable of independent operation. In addition, the Nested Vectored Interrupt Controller (NVIC) contains the functionality of comparing priority between interrupt requests and the current priority level so that nested interrupts can be handled automatically. Moreover, the power management unit is employed in order to reduce the power consumption.

B.1.2 2-phase non-overlapping clock scheme

To accomplish the data transfer in one clock cycle, the two-phase non-overlapping clock scheme, as shown in Fig.B.2, is generated internally from a single input clock signal. The read/write signals are prepared in the phase A, the read/write operations are finished in the phase B.

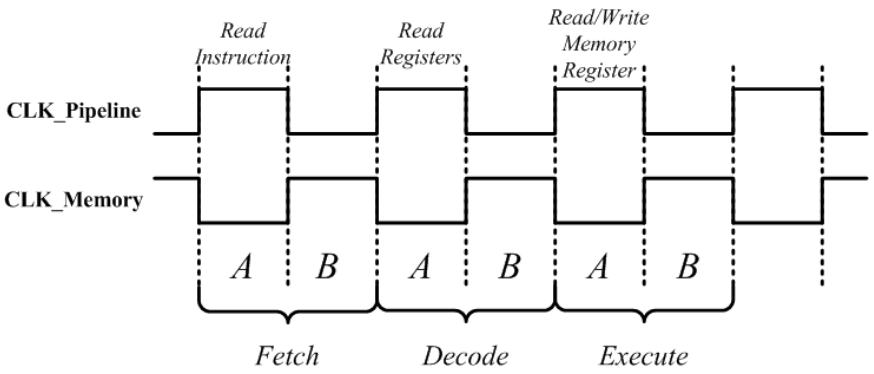

Fig. B.2: 2-phase non-overlapping clock scheme

B.1.3 Programming Model

As shown in Fig.B.3, two algorithms, adaptive impedance matching algorithm (IRQ-1) and adaptive 4-phase clock algorithm (IRQ-0), have been programmed in the Cortex-M0 processor. Furthermore, the IRQ-0 has a higher priority. If both IRQ-0 and IRQ-1 are not required, the processor will enter sleep mode. These two algorithms will be discussed in the following chapter and the corresponding assembly codes are shown in Appendix B.

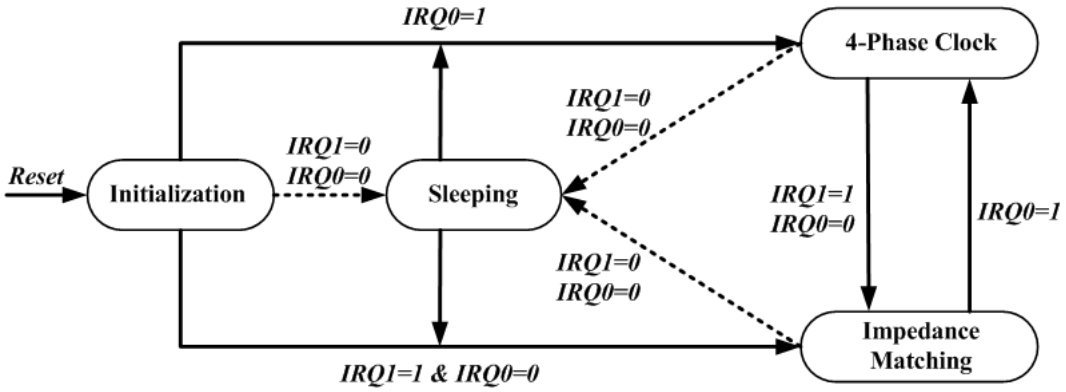

Fig. B.3: The programming model of micro-controller

B.2 Assembly Code Optimization

This section presents three criteria to evaluate the performance of assembly code. (1) Total number of instructions (related to the memory size). (2) Total number of clock cycles (related to the running time of program). (3) Types of instructions (related to the complexity of system). To improve the performance of single step algorithm, the optimized assembly code is shown in Appendix B. The running time of program is calculated by (B.1).

$$RunningTime = \frac{Numof Iter \times ClkCycles}{OperatingFreq} \tag{B.1}$$

The comparison of three assembly codes is shown in Fig.B.4. In contrast to the assembly code generated by IAR, the optimized assembly code can reduce the memory size by 36% and running time by 57%. Furthermore, the running time of single step algorithm is increased exponentially, whereas the running time of binary search algorithm is increased linearly.

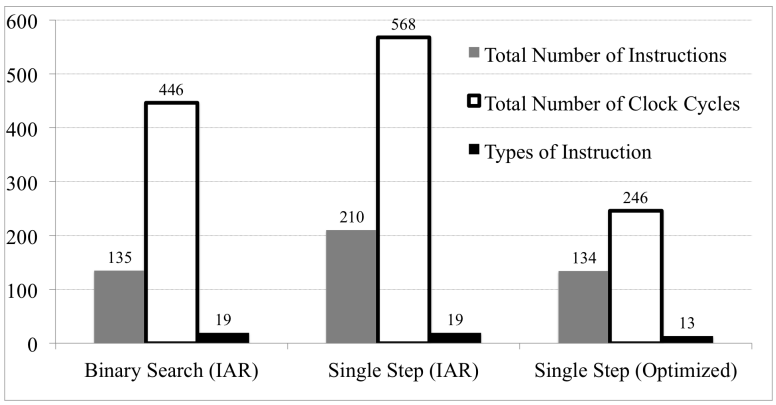

Fig. B.4: Comparison of Assembly Codes

B.3 FPGA Platform for Cortex-M0 Processor

The Xilinx Virtex-5 FPGAs has been used for demonstrating the operations of Cortex-M0 processor. The ML505 board has a 16-character, 2-line LCD, which can be used to display text information. Therefore, the block diagram of the verification platform is shown by

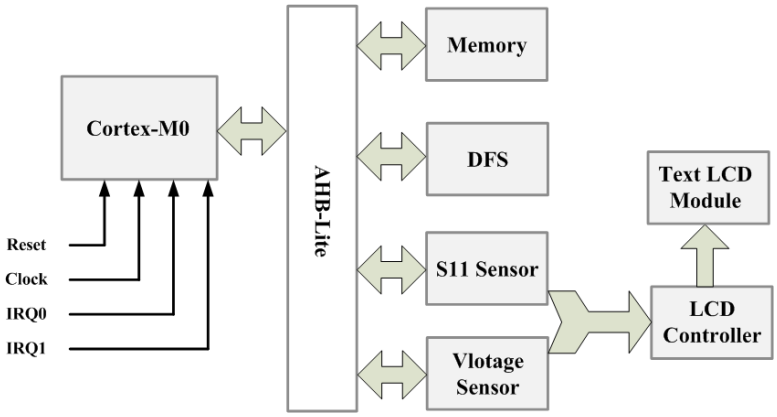

Fig. B.5: Cortex-M0 processor verification platform

The input clock signal of Cortex-M0 is connected to the crystal oscillator socket (AH15) on board, which is populated with a 100-MHz oscillator and is powered by the 3.3V supply. The device utilization report is shown by

Tab. B.1: Device utilization summary

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	1144	69120	1%
—Number used as Flip Flops	1141		
—Number used as Latch-thrus	3		
Number of Slice LUTs	3211	69120	4%
—Number used as Logic	3208		
—Number used as exclusive route-thru	3		
Number of occupied slices	1168	17280	6%
Number of LUT Flip Flop pairs used	3638		
—Number with an unused Flip Flop	2494	3638	68%
—Number with an unused LUT	427	3638	11%
—Number of fully used LUT-FF pairs	717	3638	19%
—Number of unique control sets	93		
—Number of slice register sites...	187	68120	1%

Two programs, adaptive impedance matching algorithm and adaptive 4-phase clock algorithm, are written for running in FPGA board. The outcomes of these two programs

could be dynamically observed on the LCD while the programs are running. The photo of FPGA board and the snap-shot of 8-bit control signals (*K1*, *K2*) and clock period (*T*) are shown in Fig.B.5.

Fig. B.6: Photo of the Cortex-M0 verification platform

B.4 The ASIC Implementation of Cortex-M0 Processor

After validating the RTL model, logic synthesis is performed to map the RTL code to logic gates in the targeted foundry library (AMS H35). Logic synthesis is the process of automatically converting a given RTL to technology gates based on some design constraints. The result of the synthesis process is a Netlist. The tool used in this step is "Design Compiler" that provides fast, high-capacity synthesis, and can be easily integrated into an RTL-to-GDSII design flow.

The synthesized netlist should be simulated using the same test vectors used to validate the RTL. In addition, Formal Verification software can be used to compare two given circuit descriptions. The goal of formal verification is to ensure the equivalence of two given circuit descriptions. Any simulation or formal verification errors need to be resolved since this may indicate a problem with the library of hardware components used by the synthesizer, a synthesis error, or improperly written RTL. The tool used to verify Logic Equivalence in this design is "Formality".

Synthesis tools typically have little access to place and route data for the design. With little access to physical design data, synthesis tools can miss timing goals. Hence it is important that the synthesized design exceeds the final timing requirements.

In accordance with chapter 3, the Cortex-M0 only needs to carry out the adaptive 4-phase clock algorithm and adaptive impedance matching algorithm. Hence, unused instructions are removed. As shown in Table 4.2, the operating frequency is increased from 40MHz to 60MHz and cell area is reduced from 1.77mm^2 to 0.89mm^2.

Tab. B.2: Synthesis report of Cortex-M0 processor

	20MHz	40MHz	60MHz
Standard Cortex-M0	1.77 mm^2	1.92 mm^2	X
Simplified Cortex-M0	0.89 mm^2	0.925 mm^2	1.02mm^2

Once the design has been synthesized, the physical design process can begin. The first step in the physical design process is floor planning. The Floorplan is a physical description of an ASIC. Floorplanning is a mapping between the logical description and the physical description of an ASIC. Floor planning involves partitioning the design into groupings of cells and placement of macro cells contained in the design on the chip area. Other floor planning considerations are the creation of I/O Pads and the power bussing structure.

The next step in the ASIC design flow is the Clock Tree Synthesis. Clock tree synthesis is performed in order to minimize space and power consumed by the clock signal. In this step the clock tree and clock logic is inserted and optimized. Once the clock tree is placed and optimized, the place and route can begin. The interconnect wires are routed between the library components in the netlist. After the place and route is completed, the design is checked for DRC, LVS. Finally the parasitic data gathered from the place and routed netlist is used to check if the design meets timing. The tool used to layout the design is "Cadence Encounter". The "Cadence Encounter Command File" is briefly shown in Appendix C.

The layout design certifies that the simplified Cortex-M0 core occupies 2.5mm^2. Additionally, the post-layout simulation shows that the simplified Cortex-M0 controller is capable of operating at a frequency up to 50MHz. The power consumption of Cortex-M0 controller is 16mW. However, power consumption is not a critical issue because of sleep mode. The layout of the simplified Cortex-M0 controller has been shown in Fig.B.7.

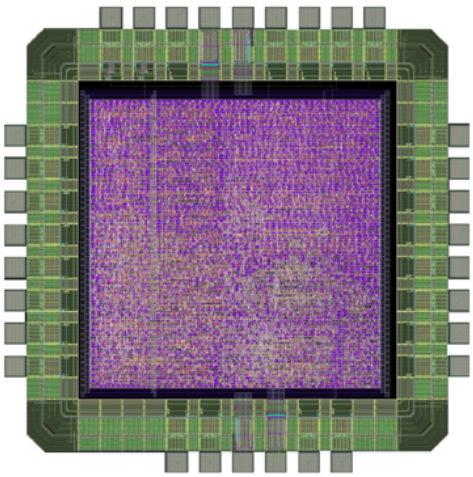

Fig. B.7: The layout of simplified Cortex-M0 controller

Tab. B.3: Assembly Code

Address	Binary Code	Assembly Code	Cycles
Main		Total Cycle: 22	
16'H0050	16'H2080	MOV R0,10000000	1
16'H0052	16'H00C0	LSL R0,3	1
16'H0054	16'H1C01	ADD R1,R0	1
16'H0056	16'H1D02	ADD R2,R0	1
16'H0058	16'H1D83	ADD R3,R6	1
16'H005A	16'H1D14	ADD R4,R2,4	1
16'H005C	16'H1D1D	ADD R5,R3,4	1
16'H005E	16'H1D26	ADD R6,R4,4	1
16'H0060	16'H1D2F	ADD R7,R5,4	1
16'H0062	16'H2032	MOV R0,50	1
16'H0064	16'H8020	STRH R0–>R4	2
16'H0066	16'H2080	MOV R0,128	1
16'H0068	16'H8030	STRH R0–>R6	2
16'H006A	16'H8038	STRH R0–>R7	2
16'H006C	16'H2000	MOV R0,0	1
16'H006E	16'H8010	STRH R0–>R2	2
16'H0070	16'HBF30	WFI	2
IRQ 0		Total Cycle:55	
16'H0080	16'H2001	MOV R0=1	1
16'H0082	16'H8010	STRH R0–>R2	2
16'H0084	16'H8821	LDRH R1<–R4	2
Address	Binary Code	Assembly Code	Cycles
16'H0086	16'H8818	LDRH R0<–R3	2
16'H0088	16'H2801	CMP R0,1	1
16'H008A	16'HD409	B{MI} label a	3
16'H008C	16'H3104	ADD R1,4	1
16'H008E	16'H2978	CMP R1,120	1
16'H0090	16'HD40D	B{MI} label b+26	3
16'H0092	16'H2178	MOV R1=120	1
16'H0094	16'H8021	STRH R1–>R4	2
16'H0096	16'H2000	MOV R0=0	1
16'H0098	16'H8010	STRH R0–>R2	2
16'H009A	16'H4770	BX	3

16'H009C	16'H3904	SUB R1,4	1
16'H009E	16'H2928	CMP R1,40	1
16'H00A0	16'HD409	B{MI} label c+18	3
16'H00A2	16'H8021	STRH R1–>R4	2
16'H00A4	16'H2000	MOV RO=0	1
16'H00A6	16'H8010	STRH RO–>R2	2
16'H00A8	16'H4770	BX	3
16'H00AA	16'H8021	STRH R1–>R4	2
16'H00AC	16'H2000	MOV R0=0	1
16'H00AE	16'H8010	STRH R0–>R2	2
16'H00B0	16'H4770	BX	3
16'H00B2	16'H2128	MOV R1=40	1
16'H00B4	16'H8021	STRH R1–>R4	2
16'H00B6	16'H2000	MOV R0=0	1
16'H00B8	16'H8010	STRH R0–>R2	2
16'H00BA	16'H4770	BX	3
IRQ 1		Total Cycle:246	
16'H00F0	16'H8828	LDRH R0<–R5	2
16'H00F2	16'H8831	LDRH R1<–R6	2
16'H00F4	16'H883A	LDRH R2<–R7	2
16'H00F6	16'H3101	ADD R1,1	1
16'H00F8	16'H29FF	CMP R1,255	1
16'H00FA	16'HD402	B{MI} PC+4	3
16'H00FC	16'HE005	B CASE2(PC+10)	3
Address	Binary Code	Assembly Code	Cycles
16'H00FE	16'H8031	STRH R1–>R6	2
16'H0100	16'H882B	LDRH R3<–R5	2
16'H0102	16'H4283	CMP R3,R0	1
16'H0104	16'HD428	B{MI} LABEL A	3
16'H0106	16'H3901	SUB R1,1	1
16'H0108	16'H8031	STRH R1–>R6	2
16'H010A	16'H3201	ADD R2,1	1
16'H010C	16'H2AFF	CMP R2,255	1
16'H010E	16'HD402	B{MI} PC+4	3
16'H0110	16'HE005	B CASE3(PC+10)	3
16'H0112	16'H803A	STRH R2–>R7	2

16'H0114	16'H882B	LDRH R3<–R5	2
16'H0116	16'H4283	CMP R3,R0	1
16'H0118	16'HD444	B{MI} LABEL B	3
16'H011A	16'H3901	SUB R1,1	1
16'H011C	16'H2900	CMP R1,0	1
16'H011E	16'HD503	B{PL} PC+6	3
16'H0120	16'H3A01	SUB R2,1	1
16'H0122	16'HE007	B PC+14	3
16'H0124	16'H8031	STRH R1–>R6	2
16'H0126	16'H3A01	SUB R2,1	1
16'H0128	16'H803A	STRH R2–>R7	2
16'H012A	16'H882B	LDRH R3<–R5	2
16'H012C	16'H4283	CMP R3,R0	1
16'H012E	16'HD453	B{MI} LABEL C	3
16'H0130	16'H3101	ADD R1,1	1
16'H0132	16'H8031	STRH R1–>R6	2
16'H0134	16'H3A01	SUB R2,1	1
16'H0136	16'H2A00	CMP R2,0	1
16'H0138	16'HD507	B{PL} PC+14	3
16'H013A	16'H2200	MOV R2,0	1
16'H013C	16'H803A	STRH R2–>R7	2
16'H013E	16'H882B	LDRH R3<–R5	2
16'H0140	16'H4283	CMP R3,R0	1
16'H0142	16'HD45A	B{MI} LABEL D	3
Address	Binary Code	Assembly Code	Cycles
16'H0144	16'H4770	BX	3
16'H0146	16'H803A	STRH R2–>R7	2
16'H0148	16'H882B	LDRH R3<–R5	2
16'H014A	16'H4283	CMP R3,R0	1
16'H014C	16'HD455	B{MI} LABEL D	3
16'H014E	16'H3201	ADD R2,1	1
16'H0150	16'H803A	STRH R2–>R7	2
16'H0152	16'H4770	BX	3
16'H0154	16'H4618	MOV R0,R3	1
16'H0156	16'H3901	SUB R1,1	1
16'H0158	16'H8031	STRH R1–>R6	2

16'H015A	16'H3201	ADD R2,1	1
16'H015C	16'H2AFF	CMP R2,255	1
16'H015E	16'HD402	B{MI} PC+4	3
16'H0160	16'HE005	B PC+10	3
16'H0162	16'H803A	STRH R2–>R7	2
16'H0164	16'H882B	LDRH R3<–R5	2
16'H0166	16'H4283	CMP R3,R0	1
16'H0168	16'HD41C	B{MI} LABEL B	3
16'H016A	16'H3901	SUB R1,1	1
16'H016C	16'H2900	CMP R1,0	1
16'H016E	16'HD503	B{PL} PC+6	3
16'H0170	16'H3A01	SUB R2,1	1
16'H0172	16'HE007	B PC+14	3
16'H0174	16'H8031	STRH R1–>R6	2
16'H0176	16'H3A01	SUB R2,1	1
16'H0178	16'H803A	STRH R2–>R7	2
16'H017A	16'H882B	LDRH R3<–R5	2
16'H017C	16'H4283	CMP R3,R0	1
16'H017E	16'HD42B	B{MI} LABEL C	3
16'H0180	16'H3101	ADD R1,1	1
16'H0182	16'H8031	STRH R1<–R6	2
16'H0184	16'H3A01	SUB R2,1	1
16'H0186	16'H2A00	CMP R2,0	1
16'H0188	16'HD502	B{PL} PC+4	3
Address	Binary Code	Assembly Code	Cycles
16'H018A	16'HE005	B PC+10	3
16'H018C	16'H803A	STRH R2–>R7	2
16'H018E	16'H882B	LDRH R3<–R5	2
16'H0190	16'H4283	CMP R3,R0	1
16'H0192	16'HD432	B{MI} LABEL D	3
16'H0194	16'H3101	ADD R1,1	1
16'H0196	16'H8031	STRH R1–>R6	2
16'H0198	16'H3201	ADD R2,1	1
16'H019A	16'H803A	STRH R2–>R7	2
16'H019C	16'H23F6	MOV R3,00F6	1
16'H019E	16'H4718	BX R3	3

16'H01A0	16'H4618	MOV R0,R3	1
16'H01A2	16'H3901	SUB R1,1	1
16'H01A4	16'H2900	CMP R1,0	1
16'H01A6	16'HD503	B{PL} PC+6	3
16'H01A8	16'H3A01	SUB R2,1	1
16'H01AA	16'HE007	B PC+14	3
16'H01AC	16'H8031	STRH R1–>R6	2
16'H01AE	16'H3A01	SUB R2,1	1
16'H01B0	16'H803A	STRH R2–>R7	2
16'H01B2	16'H882B	LDRH R3<–R5	2
16'H01B4	16'H4283	CMP R3,RO	1
16'H01B6	16'HD40F	B{MI} LABEL C	3
16'H01B8	16'H3101	ADD R1,1	1
16'H01BA	16'H8031	STRH R1–>R6	2
16'H01BC	16'H3A01	SUB R2,1	1
16'H01BE	16'H2A00	CMP R2,0	1
16'H01C0	16'HD502	B{PL} PC+4	3
16'H01C2	16'HE005	B PC+10	3
16'H01C4	16'H803A	STRH R2–>R7	2
16'H01C6	16'H882B	LDRH R3<–R5	2
16'H01C8	16'H4283	CMP R3,R0	1
16'H01CA	16'HD416	B{MI} LABEL D	3
16'H01CC	16'H3202	ADD R2,2	1
16'H01CE	16'H803A	STRH R2–>R7	2
Address	Binary Code	Assembly Code	Cycles
16'H01D0	16'H23F6	MOV R3,00F6	1
16'H01D2	16'H4718	BX R3	3
16'H01D4	16'H4618	MOV R0,R3	1
16'H01D6	16'H3101	ADD R1,1	1
16'H01D8	16'H8031	STRH R1–>R6	2
16'H01DA	16'H3A01	SUB R2,1	1
16'H01DC	16'H2A00	CMP R2,0	1
16'H01DE	16'HD502	B{PL} PC+4	3
16'H01E0	16'HE005	B PC+10	3
16'H01E2	16'H803A	STRH R2–>R7	2
16'H01E4	16'H882B	LDRH R3<–R5	2

16'H01E6	16'H4283	CMP R3,R0	1
16'H01E8	16'HD407	B{MI} LABEL D	3
16'H01EA	16'H3901	SUB R1,1	1
16'H01EC	16'H8031	STRH R1–>R6	2
16'H01EE	16'H3201	ADD R2,1	1
16'H01F0	16'H803A	STRH R2–>R7	2
16'H01F2	16'H23F6	MOV R3,00F6	1
16'H01F4	16'H4718	BX R3	3
16'H01F6	16'H4618	MOV R0,R3	1
16'H01F8	16'H23F6	MOV R3,00F6	1
16'H01FA	16'H4718	BX R3	3

Appendix C

Cadence Encounter Command File

1. *amsDbSetup*
2. *amsUserGrid*
3. *amsDbSetup*
4. *amsUserGrid*
5. *amsSetMMMC*
6. *amsSetAnalysisView minmax {func test}*
7. *amsFloorplan peri 0.65 100*
8. *amsUserGrid*
9. *floorPlan -site standard -r 0.992461112702 0.649993 51.6 50.9 73.3 86.1*
10. *amsAddEndCaps*
11. *amsPowerFP {{VDD 20} {GND 20}}*
12. *amsPlace opt*
13. *refinePlace -checkRoute 1 -preserveRouting 1 -rmAffectedRouting 1 -swapEEQ 1 -checkPinLayerForAccess {1 2 3 4}*
14. *amsGlobalConnect both*
15. *amsPowerRoute {{VDD 20} {GND 20}}*
16. *amsCts*
17. *amsTa postCTS*
18. *amsRoute wroute*

19. *amsFillperi*
20. *amsFillcore*
21. *amsTa postRoute*
22. *editFixWideWires*
23. *optDesign -postRoute*
24. *amsWrite final*
25. *amsWriteSDF4View* $\{func\_min\ func\_max\}$
26. *verifyGeometry*
27. *verifyConnectivity -type all -error 1000 -warning 50*

Appendix D

Further Discussion: Convergence Criteria

As shown in Fig.D.1, if the convergence criteria are not satisfied, a peak could be covered by the overlapping area. Therefore, the objective function is multimodal.

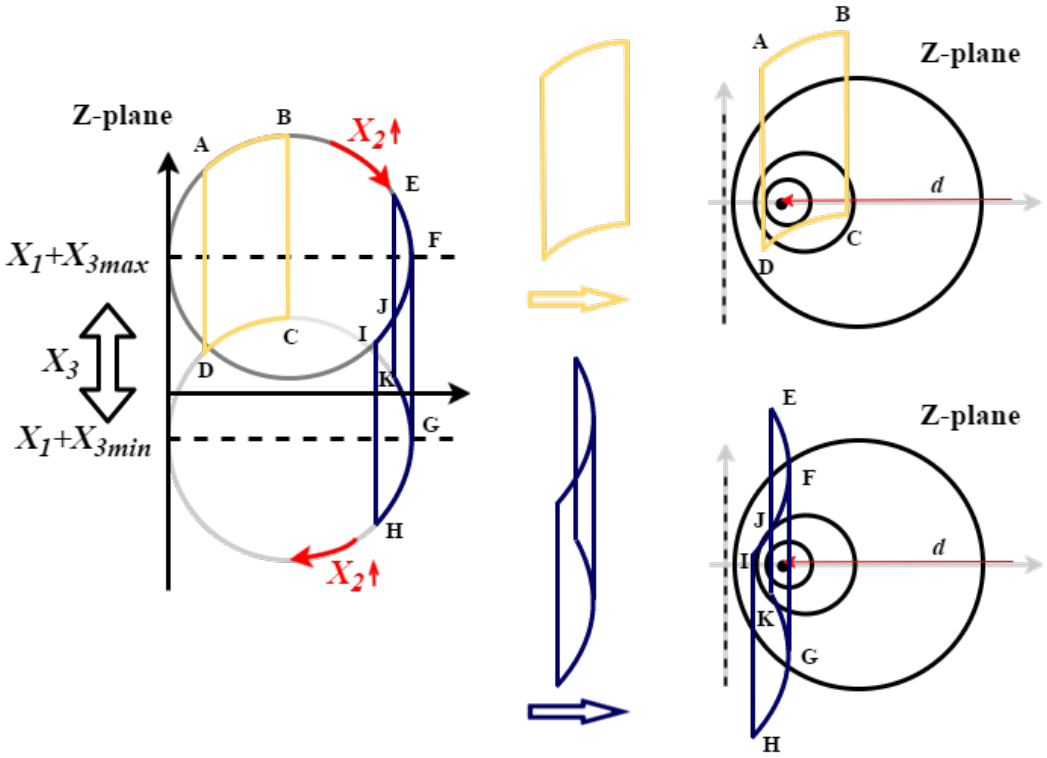

Fig. D.1: The overlapping region results in a multimodal function

If the convergence criteria are satisfied, the mapping between $\{X_2, X_3\}$ and $\{R_{in}, X_{in}\}$ is described in Fig.D.2. The image of a small black square can be estimated by a parallelogram. Therefore, the relationship between $\{X_2, X_3\}$ and $\{R_{in}, X_{in}\}$ (D.1) can be estimated by (D.2).

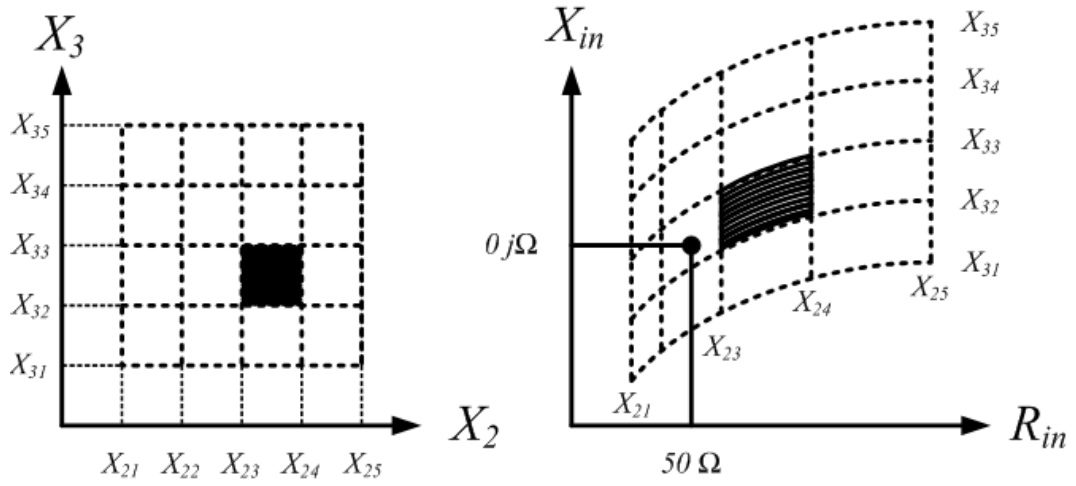

Fig. D.2: The mapping between *X* domain and *Z* domain

$$\begin{cases} R_{in} = \frac{R_L X_1^2}{R_L^2 + (X_L + X_1 + X_2)^2} \\ X_{in} = X_1 + X_3 - \frac{X_1^2 (X_L + X_1 + X_2)}{R_L^2 + (X_L + X_1 + X_2)^2} \end{cases} \tag{D.1}$$

$$\begin{bmatrix} \widetilde{R}_{in} \\ \widetilde{X}_{in} \end{bmatrix} = A \begin{bmatrix} X_2 \\ X_3 \end{bmatrix} + B \tag{D.2}$$

In accordance with section 3.3, the S_{11} is a unimodal function of $\{R_{in}, X_{in}\}$ over a convex set *T*. Therefore, the optimum point *Q1* is located at the boundary of *T* if and only if the matching point $\{Q0 : R_{in} = 50, X_{in} = 0\}$ is not covered by the convex set *T*.

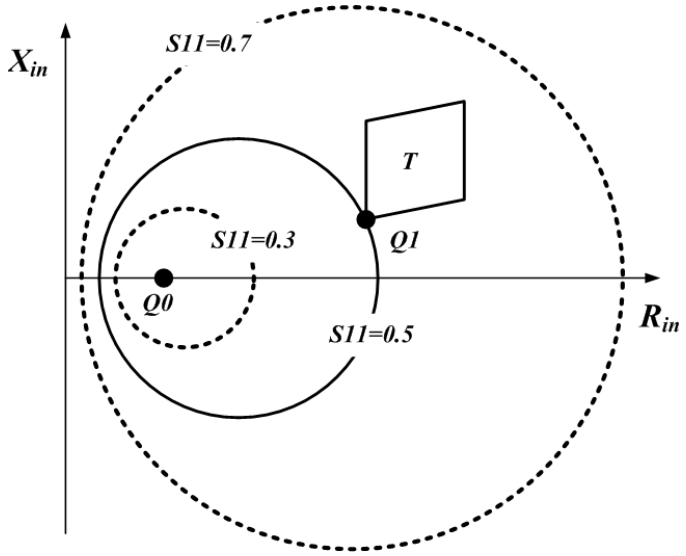

Fig. D.3: The quasiconvex function over a convex set

As shown in Fig.D.4, a straight line ABC in *X*-domain is mapped into a curve $A_1B_1C_1$ and a straight line $A_2B_2C_2$ in *Z*-domain by (D.1) and (D.2), respectively.

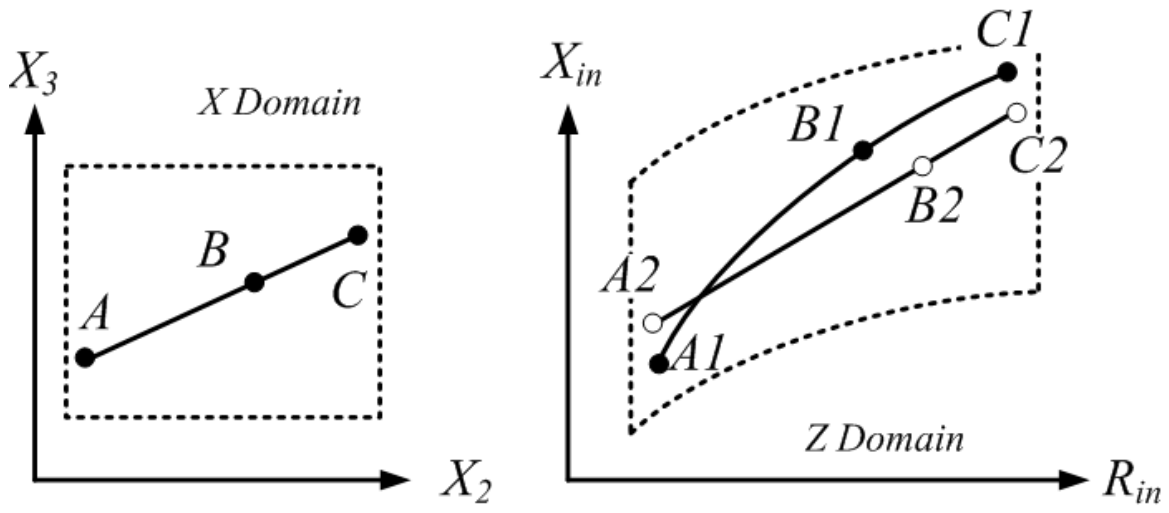

Fig. D.4: Estimation method

Jensens inequality: *A function f is quasiconvex if and only if dom f is convex and for* $\forall x, y \in dom f$ *and* $0 \leq \theta \leq 1$, $f(\theta x + (1-\theta)y) \leq max\{f(x), f(y)\}$. *[Boyd, Vandenberghe, Convex Optimization, Page 98]*

$$S_{11}(B_2) \leq max\{S_{11}(A_2), S_{11}(C_2)\} \tag{D.3}$$

The S_{11} values at points A_1,B_1,and C_1 can be estimated by (D.4).

$$\begin{cases} S_{11}(A) = S_{11}(A_1) \approx S_{11}(A_2) + S'_{11}d(A_1, A2) \\ S_{11}(B) = S_{11}(B_1) \approx S_{11}(B_2) + S'_{11}d(B_1, B2) \\ S_{11}(C) = S_{11}(C_1) \approx S_{11}(C_2) + S'_{11}d(C_1, C2) \end{cases} \tag{D.4}$$

If the points A_1,B_1,and C_1 are away from the matching point, the first derivative of S_{11} is negligible. Therefore, $S_{11}(B) \leq max\{S_{11}(A), S_{11}(C)\}$. The S_{11} is a quasiconvex function over a small region in *X*-domain, which is away from the matching point. The optimum point can be reached at the boundary of each small region. Subsequently, the search process is started from the following small region. In other words, we will converge to the neighbourhood of matching point with high probability, which can be used in the practical engineering.

List of Own Publications

[1] **Botao Xiong**, Klaus Hofmann, *'Binary search algorithm for adaptive impedance matching network'*, **Electronics Letters**, DOI: 10.1049/el.2015.3830, Volume:52, Issue:9, pp: 714-716, 21 April 2016.

[2] **Botao Xiong**, Klaus Hofmann, *'Unimodal Criteria of Tunable Matching Network'*, **Electronics Letters**, DOI: 10.1049/el.2016.0860, Volume:52, Issue:13, pp: 1149-1151, 23 June 2016.

Supervised Theses

[1] **Tian Xia**, *'ARM-based tunable impedance matching network'*, **Master Thesis, May 2015**.

[2] **Prajwal Chandrappa**, *'Optimization of 4-phase clock for high voltage charge pump'*, **Master Thesis, March 2015**.

[3] **Thanh Tiep Tra**, *'A hardware implementation of the Fast Fourier Transform'*, **Bachelor Thesis, Feb 2015**.

[4] **Lukas Jager**, *'AES with error detection using differential characteristics on an FPGA'*, **Bachelor Thesis, March 2014**.

Curriculum Vitae

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Year	*Degree*	*Institute*
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